CH7016A SDTV / HDTV Encoder

Features

- VGA to SDTV conversion supporting graphics resolutions up to 1024x768
- Analog YPrPb output for HDTV
- HDTV support for 480p, 576p, 720p, 1080i and 1080p
- Programmable digital input interface supporting RGB and YCrCb input data formats
- True scale rendering engine supports under-scan in all TV output resolutions
- Text enhancement filter
- Adaptive flicker filter with up to 7 lines of filtering
- Interlaced to progressive scan conversion for DVD
- Support for NTSC, PAL and HDTV formats
- Support for SCART connector
- Outputs CVBS, S-Video, RGB and YPrPb
- Support for Wide Screen Signaling (WSS)
- TV / Monitor connection detect
- Programmable power management
- Four 10-bit video DAC outputs
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device
- Offered in a 48-pin LQFP package

GENERAL DESCRIPTION

The CH7016A is a Display Controller device which accepts a digital graphics input signal, and encodes and transmits data through a 10-bit high speed DAC. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL TV standards (SDTV), as well as analog HDTV interface standards and graphics standards up to UXGA. The device accepts data over one 12-bit wide variable voltage data port which supports 5 different data formats including RGB and YCrCb.

The TV-Out processor will perform non-interlace to interlace conversion with scaling and flicker filter, and encode data into any of the NTSC or PAL video standards. The scaling and flicker filter is adaptive and programmable to enable superior text display. Eight graphics resolutions are supported up to 1024 by 768 with full vertical and horizontal under-scan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. ITU-R BT.656 interlaced video can also be input and scan converted to non-interlaced video.

In addition to TV encoder modes, bypass modes are included which perform color space conversion to HDTV standards and generate and insert HDTV sync signals, or output VGA style analog RGB for use as a CRT DAC.

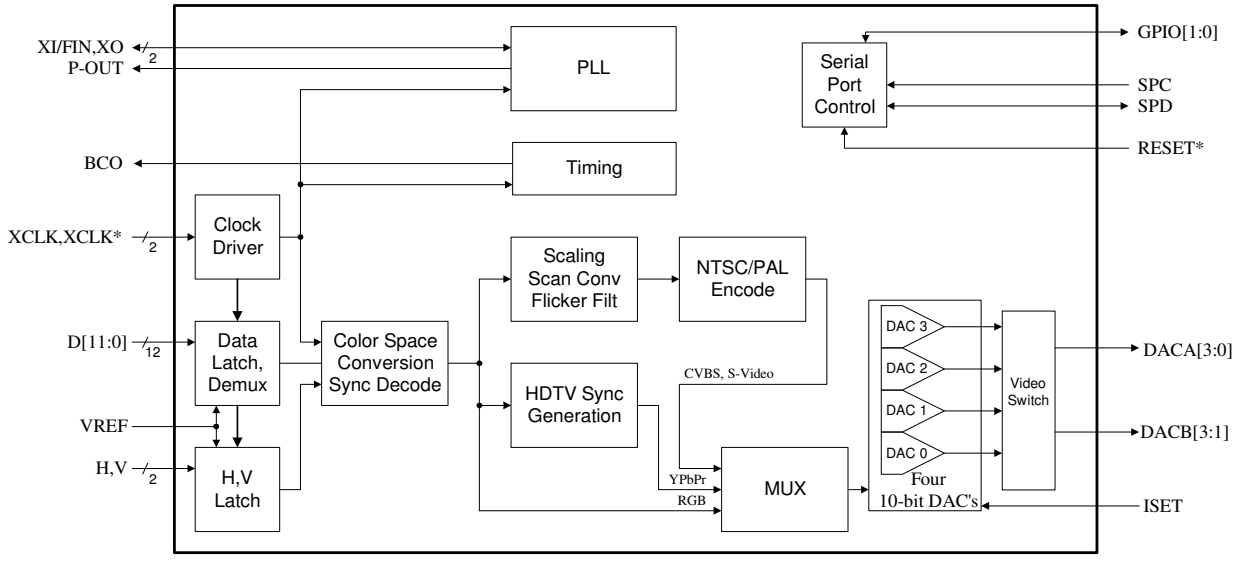

Figure 1: Functional Block Diagram

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1.0 PIN-OUT

1.1 Package Diagram

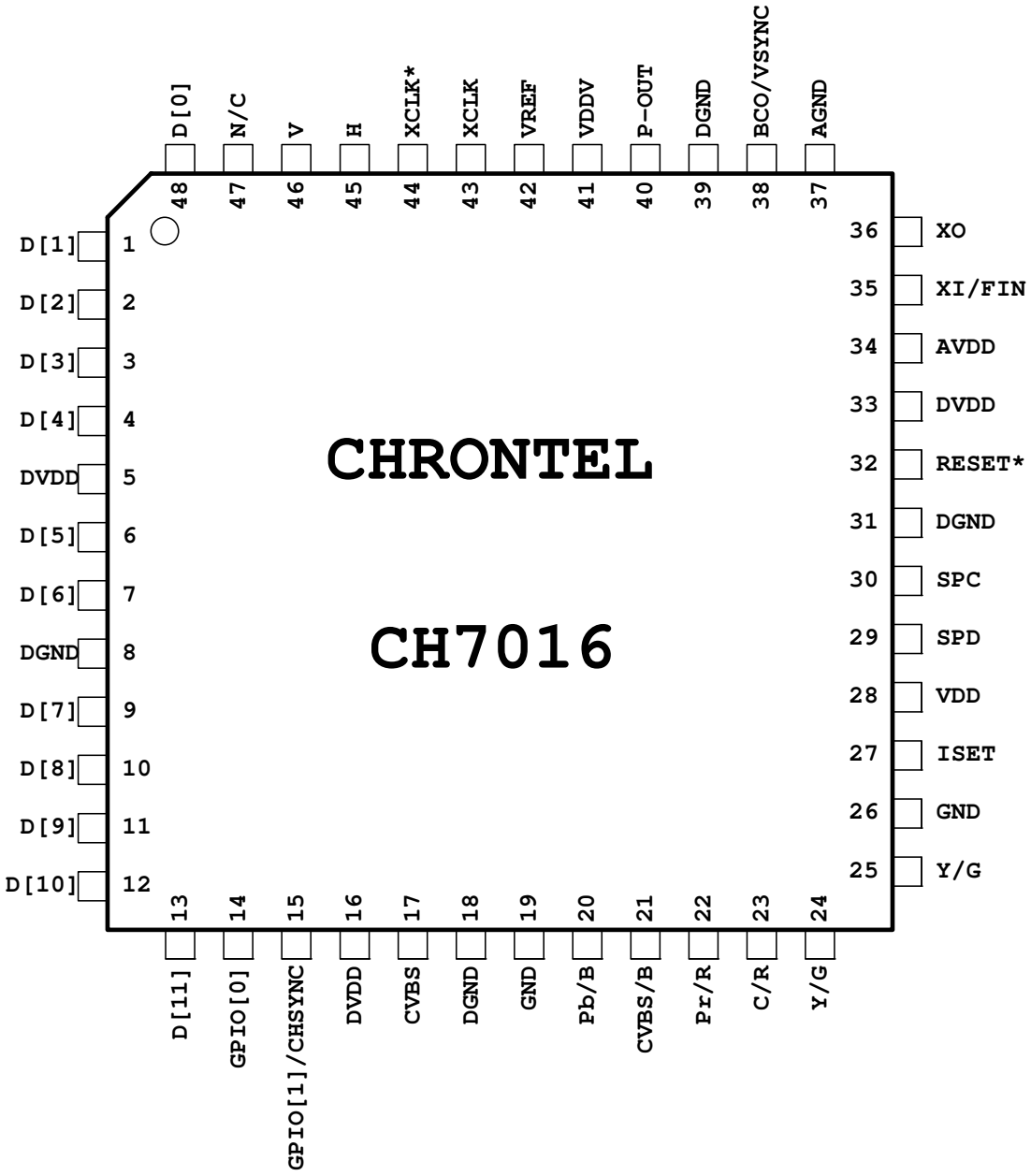

Figure 2: 48-Pin LQFP Package

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1-4, 6,7, 9-13, 48	In	D[11]-D[0]	**Data[11] through Data[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV, and the VREF signal is used as the threshold level.
14	In/Out	GPIO0	**General Purpose Input – Output0** (weak internal pull-up) This pin provides general purpose I/O controlled via the serial port. This allows an external switch to be used to select NTSC or PAL at power-up. The internal pull-up will be to the DVDD supply.
15	In/Out	GPIO1 / CHSYNC	**General Purpose Input – Output1** (weak internal pull-up) This pin provides general purpose I/O controlled via the serial port. This allows an external switch to be used to select NTSC or PAL at power-up. The internal pull-up will be to the DVDD supply. It can also be configured to output composite or horizontal sync.
17	Out	CVBS (DAC3)	**Composite Video** This pin outputs a composite video signal capable of driving a 75 ohm doubly terminated load. During bypass modes this output is valid only if the data format is compatible with one of the TV-Out display modes.
20	Out	Pb/B (DACB0)	**Pb / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to the Pb component of YPrPb or blue (for VGA bypass).
21	Out	CVBS/B (DACA0)	**Composite Video / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be composite video or blue (for SCART type 1 connections).
22	Out	Pr/R (DACB2)	**Pr / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be the Pr component of YPrPb or red (for VGA bypass)
23	Out	C/R (DACA2)	**Chroma / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video chrominance or red (for SCART type 1 connections).
24	Out	Y/G (DACB1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be the luminance component of YPrPb or green (for VGA bypass)
25	Out	Y/G (DACA1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video luminance or green (for SCART type 1 connections).
27	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 147 ohm, 1% tolerance resistor should be connected between this pin and GND (pin 24 or 26) using short and wide traces.
29	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to VDDV. Outputs are driven from 0 to VDDV. The serial port addresses for the CH7016A is 75h.
30	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port and operates with inputs from 0 to VDDV.
32	In	RESET*	**Reset * Input** (Internal pull-up) When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
35	In	XI / FIN	**Crystal Input / External Reference Input** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI/FIN input.

Table 1: Pin Description *(continued)*

Pin #	Type	Symbol	Description
36	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
38	Out	BCO	**Buffered Clock Output** This output pin provides selectable, buffered clocks to be output, driven by the DVDD supply. The output clock can be selected using the BCO Register. The levels are 0 to DVDD.
40	Out	P-Out	**Pixel Clock Output** This pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output is selectable between 1X and 2X of the pixel clock frequency. The output driver is driven from the VDDV supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
42	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
43, 44	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The clock polarity used can be selected by the MCP control bit.
45	In/Out	H	**Horizontal Sync Input / Output** When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDV, and the VREF signal is used as the threshold level. This pin must be used as an input in all bypass modes. When the SYO control bit is high, the device will output a horizontal sync pulse, 64 pixels wide. The output is driven from the DVDD supply. This output is valid with TV-Out operation.
46	In/Out	V	**Vertical Sync Input / Output** When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDV, and the VREF signal is used as the threshold level. This pin must be used as an input in all bypass modes. When the SYO control bit is high, the device will output a vertical sync pulse one line wide. The output is driven from the DVDD supply. This output is valid with TV-Out operation.
5,16,33	Power	DVDD	**Digital Supply Voltage** (3.3V)
8,18,31,39	Power	DGND	**Digital Ground**
41	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
34	Power	AVDD	**PLL Supply Voltage** (3.3V)
37	Power	AGND	**PLL Ground**
28	Power	VDD	**DAC Supply Voltage** (3.3V)
19,26	Power	GND	**DAC Ground**

2.0 FUNCTIONAL DESCRIPTION

2.1 Modes of Operation

The CH7016A is capable of being operated as a VGA to TV encoder, an ITU-R BT.601/656 encoder (with or without a de-interlacing function), or in one of several bypass modes for driving monitors requiring component video signals (HDTV, multi-sync monitors, etc.). All modes make use of the same set of DACs, and therefore cannot be used simultaneously. **Table 2** describes the possible operating modes. A 'p' following a number in the Input Scan Type column indicates a progressive scan (non-interlaced) input where the number indicates the active number of lines per frame. An 'i' following a number in the Input Scan Type column indicates an interlaced input where the number indicates the active number of lines per frame. Detailed descriptions of each of the operating modes follow **Table 2**.

Table 2: Operating Modes

Input Scan Type	Input Data Format	Output scan Type	Output Format	Operating Mode	Described In section
non-interlaced	RGB	non-interlaced	RGB	RGB bypass	2.1.5
non-interlaced (480p, 576p, 720p)	RGB / YCrCb[1]	non-interlaced	YPbPr[2,3]	HDTV/EDTV bypass	2.1.4
non-interlaced (VGA -> XGA)	RGB / YCrCb[1]	Interlaced	CVBS, S-Video	VGA to SDTV encoder (NTSC / PAL)	2.1.1
non-interlaced (VGA -> XGA)	RGB / YCrCb[1]	Interlaced	CVBS, RGB	VGA to SDTV encoder (SCART format)	2.1.1
Interlaced (1080i)	RGB / YCrCb[1]	Interlaced	YPbPr[3]	HDTV/EDTV bypass (1080i)	2.1.4
non-interlaced (1080p)	RGB / YCrCb[1]	non-interlaced	YPbPr[3]	HDTV/EDTV bypass (1080p)	2.1.4
interlaced (480i, 576i)	RGB / YCrCb[1]	non-interlaced	YPbPr[2]	ITU-R BT.601/656 TV Deinterlace (480p, 576p generation)	2.1.3
interlaced (480i, 576i)	RGB / YCrCb[1]	Interlaced	CVBS, S-Video	ITU-R BT.601/656 TV Encoder (NTSC / PAL)	2.1.2
interlaced (480i, 576i)	RGB / YCrCb[1]	Interlaced	CVBS, RGB	ITU-R BT.601/656 TV Encoder (SCART format)	2.1.2
interlaced (480i, 576i)	RGB / YCrCb[1]	Interlaced	YPbPr[2]	ITU-R BT.601/656 TV Encoder	2.1.2

[1] YCrCb signal has the following characteristics (assumed to be gamma corrected):

Y = 77/256 * R + 150/256 * G + 29/256 * B

Cr = 131/256 * R – 110/256 * G – 21/256 * B + 128

Cb = - 44/256 * R – 87/256 * G + 131/256 * B + 128

Data is 8-bit wide ITU-R BT.656 format

Data Sequence is $Cb_0Y_0Cr_0Y_1Cb_2Y_2Cr_2Y_3$

where $Cb_0Y_0Cr_0$ are co-sited samples, and Y_1 is the following luma sample

[2] YPrPb signal has the following characteristics (according to SMPTE 293M):

Y = 0.299 * R + 0.587 * G + 0.114 * B

Pb = 0.56433 * (B – Y)

Pr = 0.71327 * (R – Y)

Bi / Tri level sync inserted on each analog component

[3] YPrPb signal has the following characteristics (according to SMPTE 274M, 295M, 296M):

Y = 0.2126 * R + 0.7154 * G + 0.0722 * B

Pb = 0.53891 * (B – Y)

Pr = 0.63500 * (R – Y)

Bi / Tri level sync inserted on each analog component

2.1.1 VGA to SDTV Encoder

In VGA to SDTV Encoder mode non-interlaced data, sync and clock signals are input to the device from a graphics controllers digital output port. A clock signal (P-Out) can be output as a frequency reference to the graphics controller, which is recommended to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the device from the graphics controller, but can be embedded into the data stream in YCrCb input data formats, or can be output to the graphics controller. Data is 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. Input data will be scaled, scan converted and flicker filtered, then encoded into the selected video standard and output from the video DACs. NTSC and PAL formats are supported. The device can output data in S-Video and CVBS format, or as RGB for interface to a SCART connector. The graphics resolutions supported for VGA to TV output are shown in **Table 3** below. As the table shows, the amount of scaling is programmable. The flicker filter includes text enhancement circuitry, and the amount of flicker filtering and text enhancement performed is programmable, with the maximum number of taps used in the filter being five, six or seven depending upon the scaling ratio.

Table 3: VGA to TV Operating Modes

Input Resolution	Active Video Aspect Ratio	Pixel Aspect Ratio	TV Output Standard	Scaling Ratios
512x384	4:3	1:1	PAL	5/4, 1/1
512x384	4:3	1:1	NTSC	5/4, 1/1
720x400	4:3	1.35:1.00	PAL	5/4, 1/1
720x400	4:3	1.35:1.00	NTSC	5/4, 1/1, 25/21
640x400	8:5	1:1	PAL	5/4, 1/1
640x400	8:5	1:1	NTSC	5/4, 1/1, 7/8, 25/21
640x480	4:3	1:1	PAL	5/4, 1/1, 5/6, 25/21
640x480	4:3	1:1	NTSC	1/1, 7/8, 5/6
720x480	4:3	9:8	NTSC	1/1, 7/8, 5/6
720x576	4:3	15:12	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	NTSC	3/4, 7/10, 5/8
1024x768	4:3	1:1	PAL	5/7, 5/8, 5/9
1024x768	4:3	1:1	NTSC	5/8, 5/9, 1/2

2.1.2 ITU-R BT.601/656 TV Encoder

In ITU-R BT.601/656 TV Encoder mode, interlaced data, sync and clock signals are input to the CH7016A from a graphics controllers digital output port, or the output of an MPEG decoder device. The YCrCb data format is most commonly used in these modes, but RGB data can be used as well. A clock signal (P-Out) can be output as a frequency reference to the graphics device. Horizontal and vertical sync signals are normally sent to the CH7016A from the graphics device, but can be embedded into the data stream in YCrCb input data formats, or can be output to the graphics controller. Data is 2X multiplexed, and the XCLK clock signal is 2X times the pixel rate. Input data bypasses the scaling, scan conversion and flicker filtering blocks, is encoded into the selected video standard and output from the video DACs. NTSC and PAL formats are supported. The device can output data in S-Video and CVBS format, or as RGB for interface to a SCART connector or in YPrPb format. The graphics resolutions supported for ITU-R BT.601/656 TV output are shown in **Table 4** below. The timing of the sync signals is shown in **Figure 3** below. Note that the alignment of the VSYNC signal to the HSYNC signal changes from field 1 to field 2 to allow the CH7016A to identify the correct field.

Table 4: ITU-R BT.601/656 TV Encoder Operating Modes

Input Resolution	Active Video Aspect Ratio	Pixel Aspect Ratio	TV Output Standard	Scaling Ratios
720x480i	4:3	9:8	NTSC	1/1
720x576i	4:3	15:12	PAL	1/1

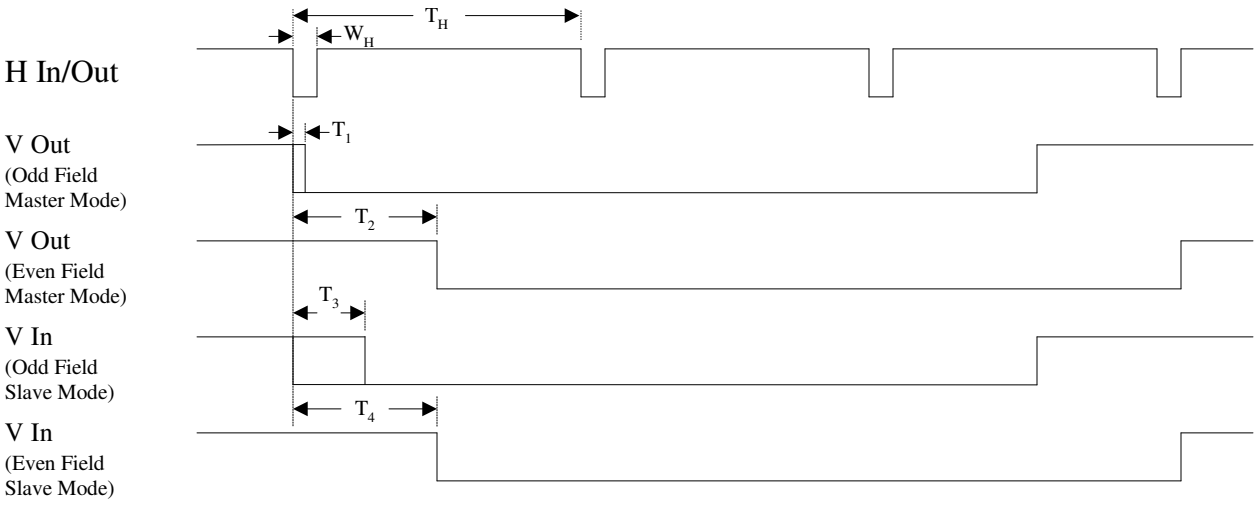

Figure 3: Interlaced Sync Input/Output Timing

Table 5: Interlaced Sync Input/Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_{PCK}	Input clock period	6.73		47.62	µs
T_H	Total Line Period				
	SDTV	63.5		63.5	µs
	HDTV	14.8		37.0	µs
W_H	Hsync Width				
	When output from CH7016A	64		64	Pixel clocks
	When input to CH7016A	1			Pixel clocks
T_1	Odd Field (Field 1) V SYNC out to H SYNC out alignment		0		µs
T_2	Even Field (Field 2) V SYNC out delay from H SYNC out		$0.5*T_H$		µs
T_3	Odd Field (Field 1) V SYNC in to H SYNC in alignment	0		$W_H - T_{PCK}$	µs
T_4	Even Field (Field 2) V SYNC in delay from H SYNC in	W_H		$T_H - T_{PCK}$	µs

2.1.3 ITU-R BT.601/656 TV De-Interlace

In ITU-R BT.601/656 TV De-Interlace mode, interlaced data, sync and clock signals are input to the CH7016A from a graphics controllers digital output port, or the output of an MPEG decoder device. The YCrCb data format is most commonly used in these modes, but RGB data can be used as well. A clock signal (P-Out) can be output as a frequency reference to the graphics device. Horizontal and vertical sync signals are normally sent to the CH7016A from the graphics device, but can be embedded into the data stream in YCrCb input data formats, or can be output to the graphics controller. Data is 2X multiplexed, and the XCLK clock signal is 2X times the pixel rate. Input data is scan converted from interlaced to non-interlaced data, color space converted to the selected video format, has sync signals generated and is output from the video DACs. The output format is YPbPr. The graphics resolutions supported for ITU-R BT.601/656 TV De-Interlace mode are shown in **Table 6** below. The timing of the sync signals is shown in **Figure 3**. Note that the alignment of the VSYNC signal to the HSYNC signal changes from field 1 to field 2 to allow the CH7016A to identify the correct field.

Table 6: ITU-R BT.601/656 TV De-Interlace Operating Modes

Input Resolution	Active Video Aspect Ratio	Pixel Aspect Ratio	TV Output Standard	Scaling Ratios
720x480i	4:3	9:8	720x480p	1/1
720x576i	4:3	15:12	720x576p	1/1

2.1.4 HDTV / EDTV Bypass

In HDTV / EDTV Bypass mode, data, sync and clock signals are input to the CH7016A from a graphics device in the scanning method that matches the display device (interlaced data is sent to the CH7016A to drive an interlaced display, non-interlaced data is sent to the CH7016A to drive a non-interlaced display). The input data format can be YCrCb or RGB. A clock signal (P-Out) can be output as a frequency reference to the graphics device. Horizontal and vertical sync signals must either be sent to the CH7016A from the graphics device or embedded in the data stream according to SMPTE standards. Data is 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. Input data is color space converted to the selected video format, has sync signals generated and is output from the video DACs. The output format is YPbPr. The graphics resolutions supported for HDTV Bypass mode are shown in **Table 7** below. The resolutions supported for EDTV Bypass mode is shown in **Table 8:**. The timing of the sync signals for interlaced input modes is shown in **Figure 3**. Note that in interlaced input modes the alignment of the VSYNC signal to the HSYNC signal changes from field 1 to field 2 to allow the CH7016A to identify the correct field. No scaling, scan conversion or flicker filtering is applied in HDTV / EDTV Bypass mode.

Table 7: HDTV Bypass

Input Resolution	Total Resolution	Scan Type	Pixel Clock (MHz)	Frame Rate (Hz)	Standard
1280x720	1650x750	Non-Interlaced	74.25 74.25/1.001	60 60/1.001	SMPTE 296M
1280x720	1648x750	Non-Interlaced	74.160	60	
1920x1080	2200x1125	Interlaced	74.25 74.25/1.001	30 30/1.001	SMPTE 274M
1920x1080	2640x1125	Interlaced	74.25	25	SMPTE 274M
1920x1080	2376x1250	Interlaced	74.25	25	SMPTE 295M
1920x1080	2200x1125	Non-Interlaced	148.5 148.5/1.001 74.25 74.25/1.001	60 60/1.001 30 30/1.001	SMPTE 274M
1920x1080	2640x1125	Non-Interlaced	148.5 74.25	50 25	SMPTE 274M
1920x1080	2750x1125	Non-Interlaced	74.25 74.25/1.001	24 24/1.001	SMPTE 274M
1920x1080	2752x1125	Non-Interlaced	74.304	24	
1920x1080	2376x1250	Non-Interlaced	148.5	50	SMPTE 295M

Table 8: EDTV Bypass

Active Resolution	Total Resolution	Scan Type	Pixel Clock (MHz)	Frame Rate (Hz)	Standard
720x480	858x525	Non-Interlaced	27.027	60	EIA-770.2-A
720x483	858x525	Non-Interlaced	27.0	60/1.001	SMPTE 293M
720x576	864x625	Non-interlaced	27.0	50	ITU-R BT.1358

2.1.5 RGB Bypass

In RGB Bypass mode, data, sync and clock signals are input to the CH7016A from a graphics device, and bypassed directly to the D/A converters to implement a second CRT DAC function. External sync signals must be supplied from the graphics device. These sync signals are buffered internally, and can be output to drive the CRT. The input data format must be RGB in this operating mode. Input data is 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The CH7016A can support a pixel rate of 165MHz. This operating mode uses 8-bits of three of the DACs 10-bit range, and provides a nominal signal swing of 0.661V (or 0.7V depending on DAC Gain setting in control registers) when driving a 75Ω doubly terminated load. No scaling, scan conversion or flicker filtering is applied in RGB Bypass modes.

2.2 TV Encoder / Bypass RGB / Component Video Outputs

Three of the four TV encoder DAC outputs can be switched to two sets of output pins DACA[2:0] and DACB[2:0] via video switches. The fourth DAC output, DAC3 is not switched so that CVBS output is available for the HDTV configuration in addition to the standard TV output configurations. This feature facilitates simple connection to two sets of video connectors as listed in **Table 9**.

Table 9: TV Output Configurations

Pin # (name)	**2 RCA + 1 S-Video**	**SCART**	
Pin 21 (DACA0)	CVBS	B	
Pin 25 (DACA1)	Y	G	
Pin 23 (DACA2)	C	R	
Pin 17 (DAC3)	CVBS	CVBS	
	VGA – Bypass RGB	**HDTV**	**SDTV** [1]
Pin 20 (DACB0)	B	Pb	Pb
Pin 24 (DACB1)	G	Y	Y
Pin 22 (DACB2)	R	Pr	Pr
Pin 17 (DAC3)			CVBS

If the application calls for CVBS/S-video, SCART, RGB and YPrPb to output on one set of DAC output pins, different reconstruction filters for each type of signal can be implemented on the breakout cables.

The TV Encoder can be bypassed and input data drives the DACs directly. This mode can go to 165MP/s. The CH7016A supports YPrPb output for driving 480i, 480p, 576i, 576p, 720p, 1080i and 1080p TV sets, and SCART RGB for European TV.

Note: CVBS is available with YPrPb for SDTV interlaced outputs.

2.3 Input Interface

2.3.1 Overview

Two distinct methods of transferring data to the CH7016A are described. They are:

- Multiplexed data, clock input at 1X the pixel rate
- Multiplexed data, clock input at 2X the pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7016A is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X pixel rate the data applied to the CH7016A is latched with one edge of the clock (also known as single edge transfer mode or SDR). The polarity of the pixel clock can be reversed under serial port control. In single edge transfer modes, the clock edge used to latch data is programmable. In dual edge transfer modes, the clock edge used to latch the first half of each pixel is programmable.

2.3.2 Input Clock and Data Timing Diagram

Figure 4 below shows the timing diagram for input data and clocks. The first XCLK/XCLK* waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK/XCLK* waveform represents the input clock for the dual edge transfer (DDR) method. The timing requirements are given in section 4.5.

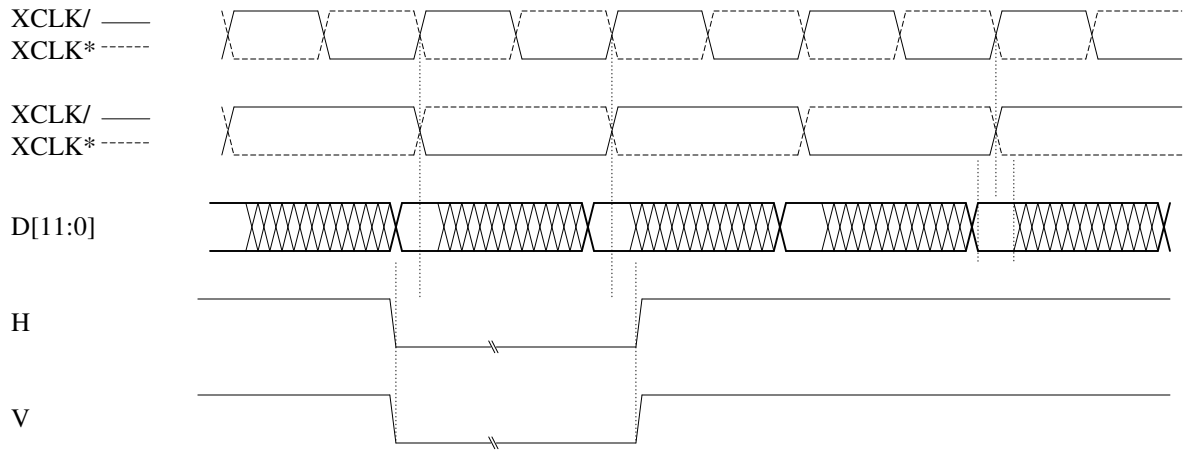

Figure 4: Clock, Data and Interface Timing

2.3.3 Data De-skew Feature

The de-skew feature allows adjustment of the input setup and hold time. The input data D[11:0] can be latched slightly before or after the latching edge of XCLK depending on the amount of the de-skew. Note that the XCLK is not changed, only the time at which the data is latch relative to XCLK. The de-skew is controlled using the XCMD[3:0] bits located in Register 1Dh. The delay t_{CD} between clock and data is given by the following formula:

t_{CD} = - XCMD[3:0] * t_{STEP} for $0 \le$ XCMD[3:0] ≤ 7
t_{CD} = (XCMD[3:0] – 8) * t_{STEP} for $8 \le$ XCMD[3:0] ≤ 15

where XCMD is a number between 0 and 15 represented as a binary code
t_{STEP} is the adjustment increment (see section 4.5)

The delay is also tabulated in **Table 31**.

2.3.4 Input Data Formats

The CH7016A supports 5 different multiplexed data formats, each of which can be used with a 1X clock latching data on both clock edges, or a 2X clock latching data with a single edge (rising or falling depending on the value of the MCP bit – rising refers to a rising edge on the XCLK signal, a falling edge on the XCLK* signal). The input data formats are (IDF[2:0]):

IDF	Description
0	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 1)
1	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 2)
2, 5	8-bit multiplexed RGB input (16-bit color, 565)
3	8-bit multiplexed RGB input (15-bit color, 555)
4	8-bit multiplexed YCrCb input (24-bit color), (Y, Cr and Cb are multiplexed)

The input data format is shown in **Figure 5** below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.; P0a and P0b) will contain a complete pixel encoded as shown in **Table 10** through **Table 13**.

It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

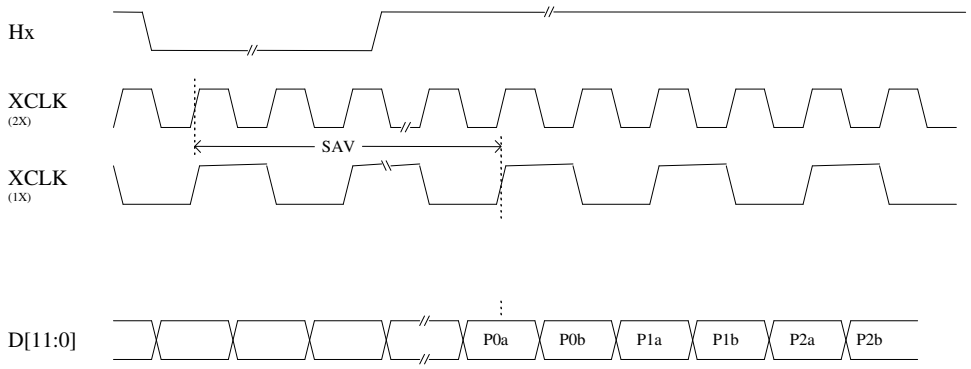

Figure 5: 12-bit Multiplexed Input Data Formats (IDFx = 0,1,2,3,4)

Table 10: Multiplexed Input Data Formats (IDF = 0, 1)

IDF = Format =		0 12-bit RGB				1 12-bit RGB			
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P0a**	**P0b**	**P1a**	**P1b**
Bus Data	D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	D[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 11: Multiplexed Input Data Formats (IDF = 2, 3)

IDF = Format =		2 RGB 5-6-5				3 RGB 5-5-5			
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P0a**	**P0b**	**P1a**	**P1b**
Bus Data	D[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	D[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	D[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	D[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	D[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	D[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	D[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	D[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 12: Multiplexed Input Data Formats (IDF = 4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P2a**	**P2b**	**P3a**	**P3b**
Bus Data	D[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

Table 13: Embedded Sync in Multiplexed Data Format (IDF=4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P2a**	**P2b**	**P3a**	**P3b**
Bus Data	D[7]	1	0	0	S[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	1	0	0	S[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	1	0	0	S[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	1	0	0	S[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	1	0	0	S[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	1	0	0	S[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	1	0	0	S[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	1	0	0	S[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

In this mode, the S[7:0] byte contains the following data:

S[6] = F = 1 during field 2, 0 during field 1
S[5] = V = 1 during field (frame) blank, 0 elsewhere
S[4] = H = 1 during EAV (synchronization reference at the end of active video)
0 during SAV (synchronization reference at the start of active video)

Bits S[7] and S[3:0] are ignored.

Table 14: Multiplexed Input Data Formats (IDF = 5)

IDF = Format =		5 RGB 5-6-5			
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**
Bus Data	D[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[2]	B0[5]	G0[7]	B1[5]	G1[7]
	D[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[0]	B0[3]	G0[5]	B1[3]	G1[5]

2.4 TV Output

2.4.1 Adaptive Flicker Filter

The CH7016A integrates an advanced 2-line, 3-line, 4-line, 5-line, 6-line and 7-line (depending on mode) vertical deflickering filter circuit to help eliminate the flicker associated with interlaced displays. This flicker circuit provides an adaptive filter algorithm for implementing flicker reduction with selections of high, medium or low flicker content for both luma and chroma channels (see register descriptions). In addition, a special text enhancement circuit incorporates additional filtering for enhancing the readability of test. These modes are fully programmable via serial port interface using the flicker filter register.

2.4.2 Color Burst Generation

The CH7016A allows the subcarrier frequency to be accurately generated from a 14.31818 MHz crystal oscillator, leaving the subcarrier frequency independent of the graphics pixel clock frequency. As a result, the CH7016A may be used with most VGA chips (with an appropriate digital interface) since the CH7016A subcarrier frequency can be generated without being dependent on the precise pixel rates of VGA controllers. This feature is important since even a ±0.01% subcarrier frequency variation is enough to cause some televisions to lose color lock.

In addition, the CH7016A has the capability to genlock the color burst signal to the VGA horizontal sync frequency, which enables a fully synchronous system between the graphics controller and the television. When genlocked, the CH7016A can stop “dot crawl” motion (for composite NTSC modes), thus eliminating the annoyance of moving borders. Both of these features are under programmable control through the register set.

2.4.3 NTSC and PAL Operation

Composite and S-Video outputs are supported in either NTSC or PAL format. The general parameters used to characterize these outputs are listed in **Table 15** and shown in **Figure 6** (see **Figure 7** through **Figure 14** for illustrations of composite and S-Video output waveforms).

ITU-R BT.470 Compliance

The CH7016A is predominantly compliant with the recommendations called out in ITU-R BT.470. The following are the only exceptions to this compliance:

- The frequencies of Fsc, Fh, and Fv can only be guaranteed in clock/sync master mode, not in clock/sync slave mode when the graphics device generates these frequencies.
- It is assumed that gamma correction, if required, is performed in the graphics device which establishes the color reference signals.
- All modes provide the exact number of lines called out for NTSC and PAL modes respectively, except mode 21, which outputs 800x600 resolution, scaled by 3:4, to PAL format with a total of 627 lines (vs. 625).
- Chroma signal frequency response will fall within 10% of the exact recommended value.
- Pulse widths and rise/fall times for sync pulses, front/back porches, and equalizing pulses are designed to approximate ITU-R BT.470 requirements, but will fall into a range of values due to the variety of clock frequencies used to support multiple operating modes.

Table 15: NTSC/PAL Composite Output Parameters

Symbol	Description	Level (mV)		Duration (µs)	
		NTSC	PAL	NTSC	PAL
A	Front Porch	287	300	1.49 - 1.51	1.48 - 1.51
B	Horizontal Sync	0	0	4.69 - 4.72	4.69 - 4.71
C	Breezeway	287	300	0.59 - 0.61	0.88 - 0.92
D	Color Burst	287	300	2.50 - 2.53	2.24 - 2.26
E	Back Porch	287	300	1.55 - 1.61	2.62 - 2.71
F	Black	340	300	0.00 - 7.50	0.00 - 8.67
G	Active Video	340	300	37.66 - 52.67	34.68 - 52.01
H	Black	340	300	0.00 - 7.50	0.00 - 8.67

For this table and all subsequent figures, key values are:

Note:

1. RSET = 147 ohms; V(ISET) = 1.235V; 75 ohms doubly terminated load. RSET is the resistor connected to the pin ISET.
2. Duration may vary slightly in different modes due to the different clock frequencies used.
3. Active video and black (F, G, H) times vary greatly due to different scaling ratios used in different modes.
4. Black times (F and H) vary with position controls.

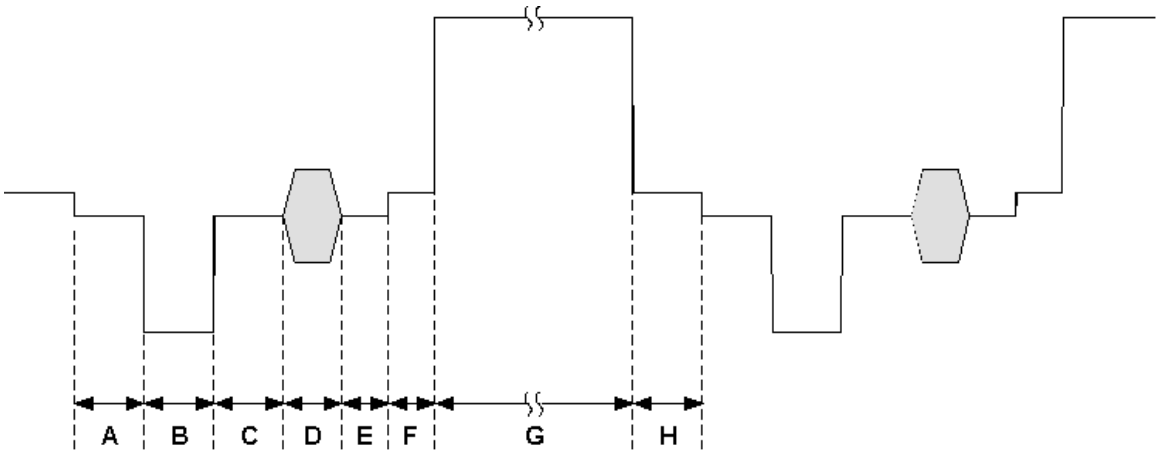

Figure 6: NTSC / PAL Composite Output

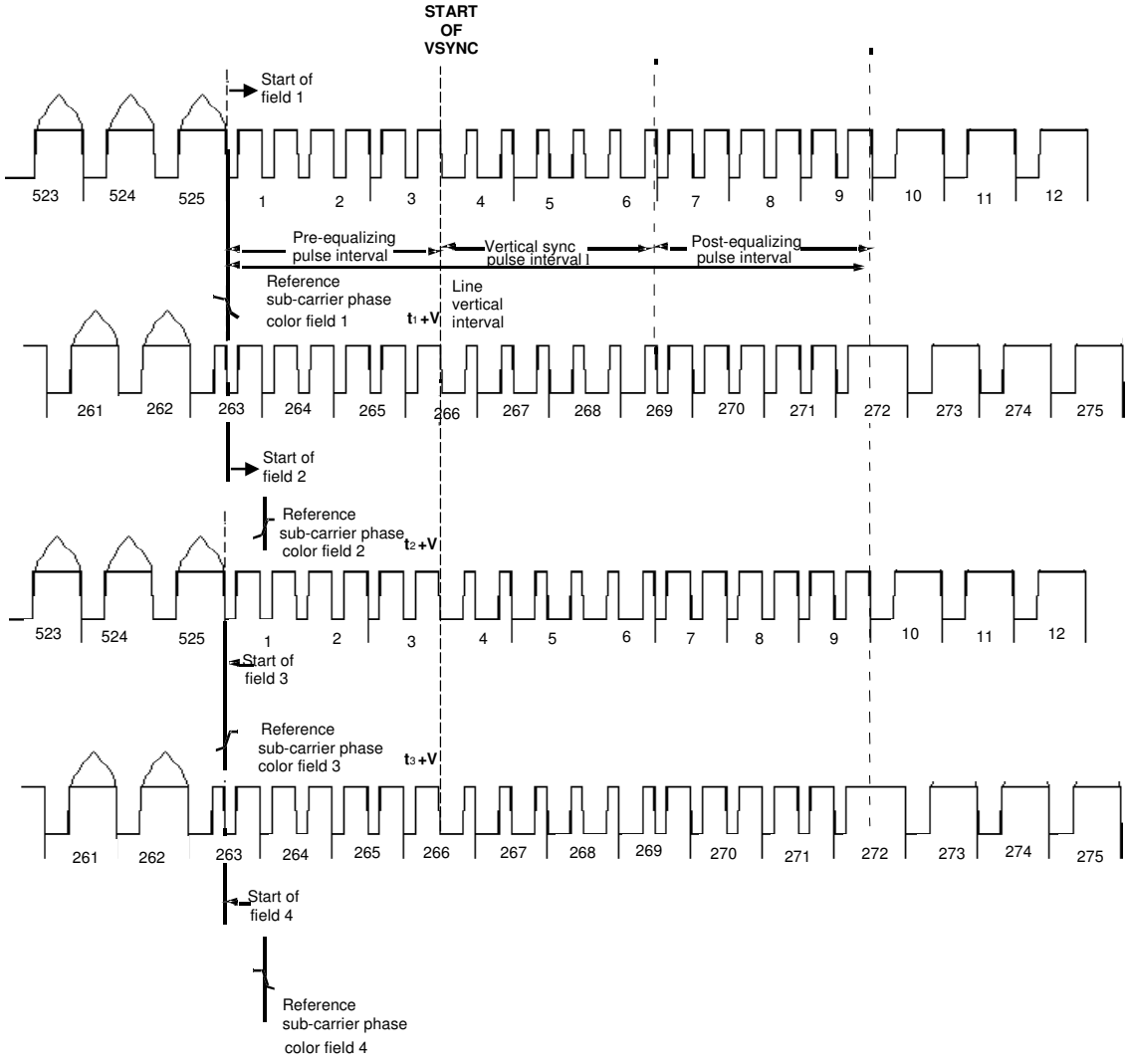

Figure 7: Interlaced NTSC Video Timing

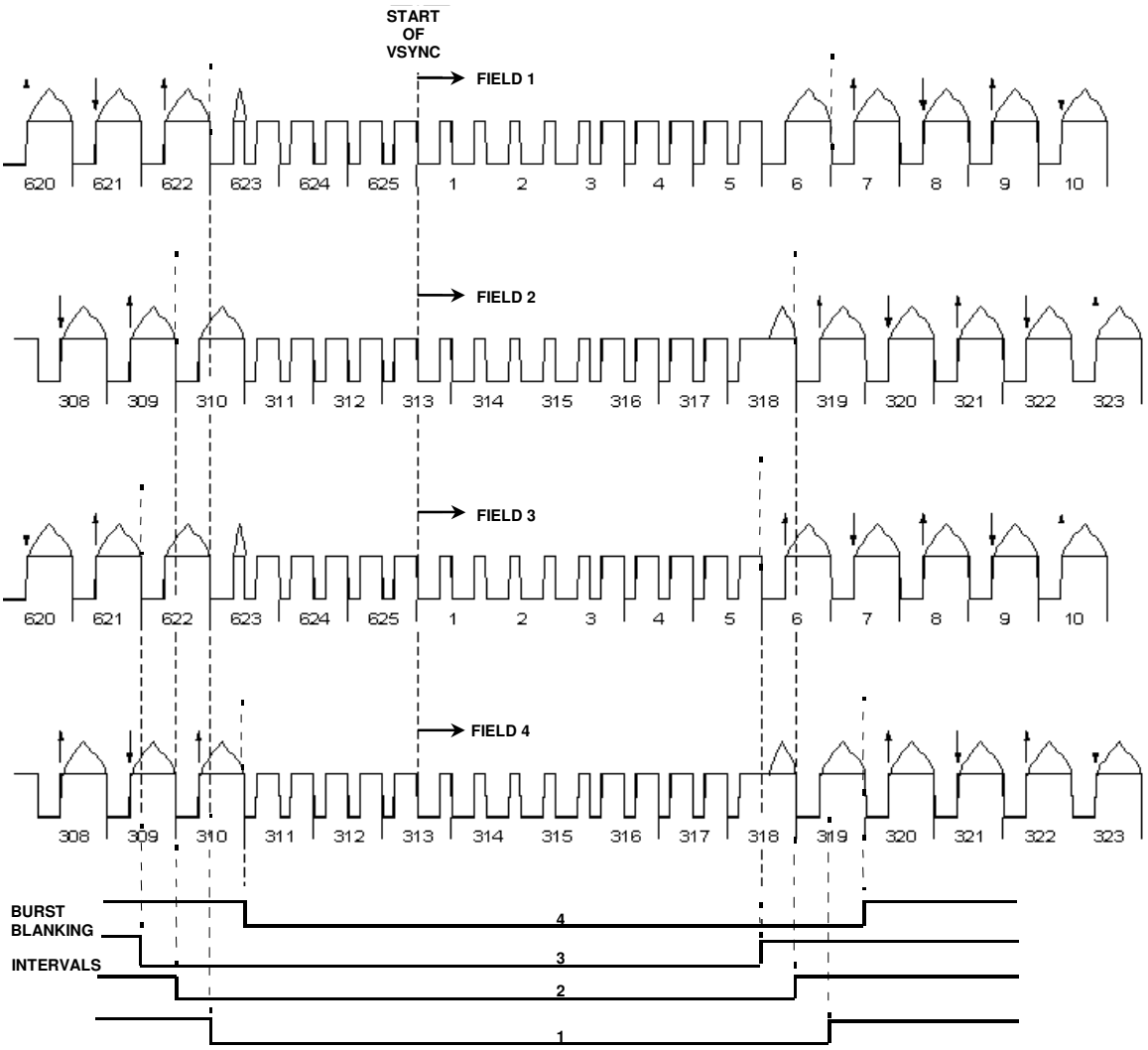

Figure 8: Interlaced PAL Video Timing

Color/Level	mA	V
White	26.66	1.000
Yellow	24.66	0.925
Cyan	21.37	0.801
Green	19.37	0.726
Magenta	16.22	0.608
Red	14.22	0.533
Blue	11.08	0.415
Black	9.08	0.340
Blank	7.65	0.287
Sync	0.00	0.000

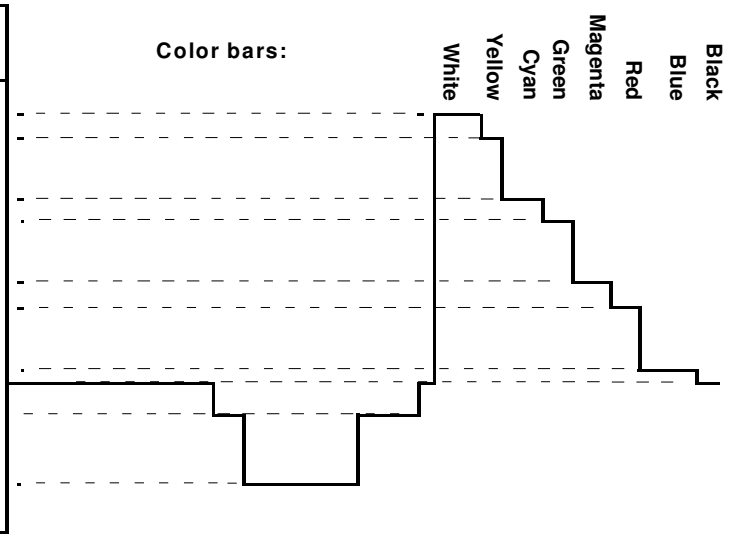

Figure 9: NTSC Y (Luminance) Output Waveform (DACG = 0)

Color/Level	mA	V
White	26.75	1.003
Yellow	24.62	0.923
Cyan	21.11	0.792
Green	18.98	0.712
Magenta	15.62	0.586
Red	13.49	0.506
Blue	10.14	0.380
Blank/ Black	8.00	0.300
Sync	0.00	0.000

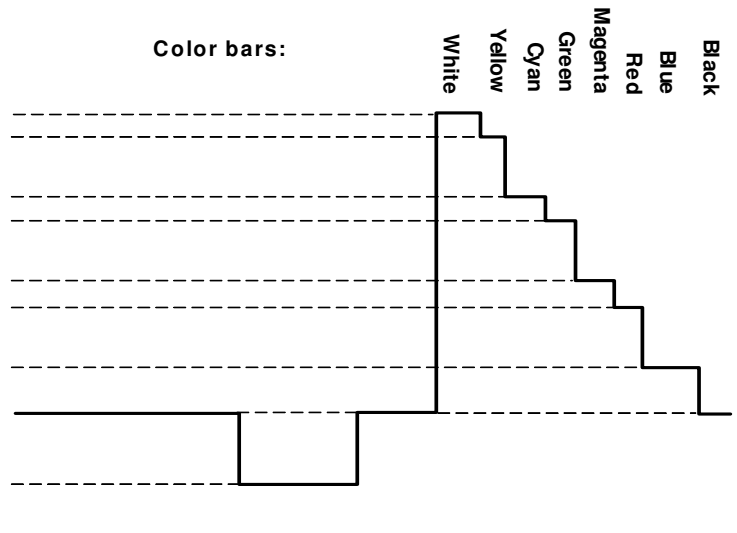

Figure 10: PAL Y (Luminance) Video Output Waveform (DACG = 1)

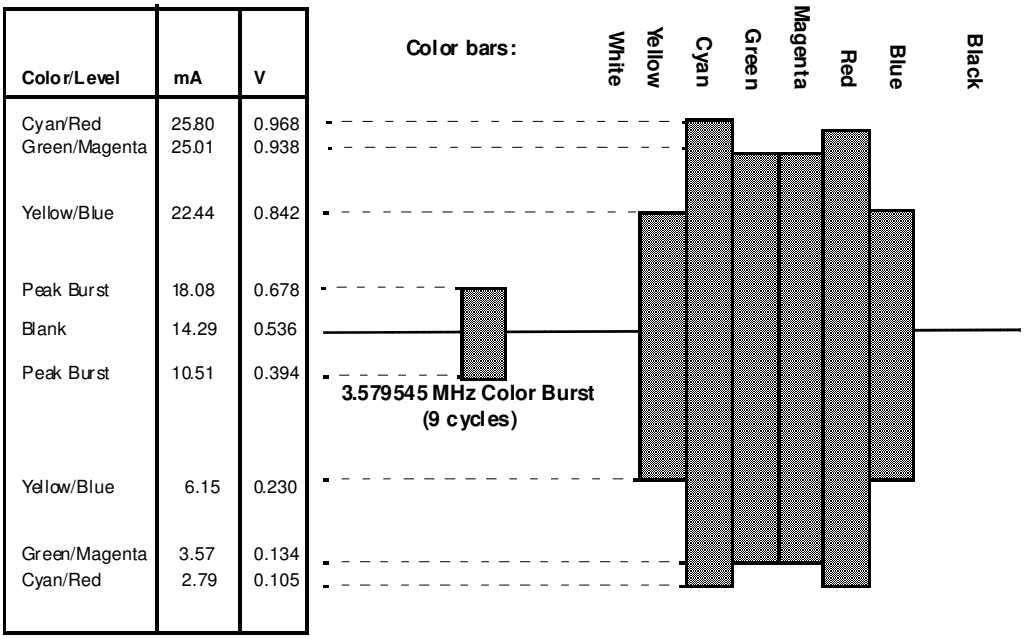

Figure 11: NTSC C (Chrominance) Video Output Waveform (DACG = 0)

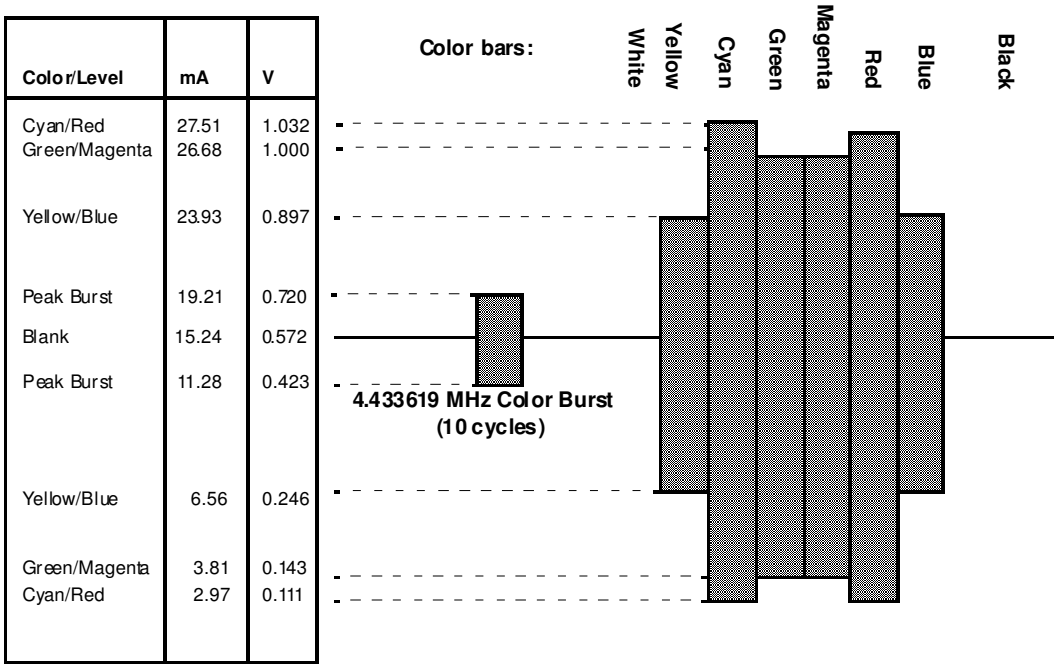

Figure 12: PAL C (Chrominance) Video Output Waveform (DACG = 1)

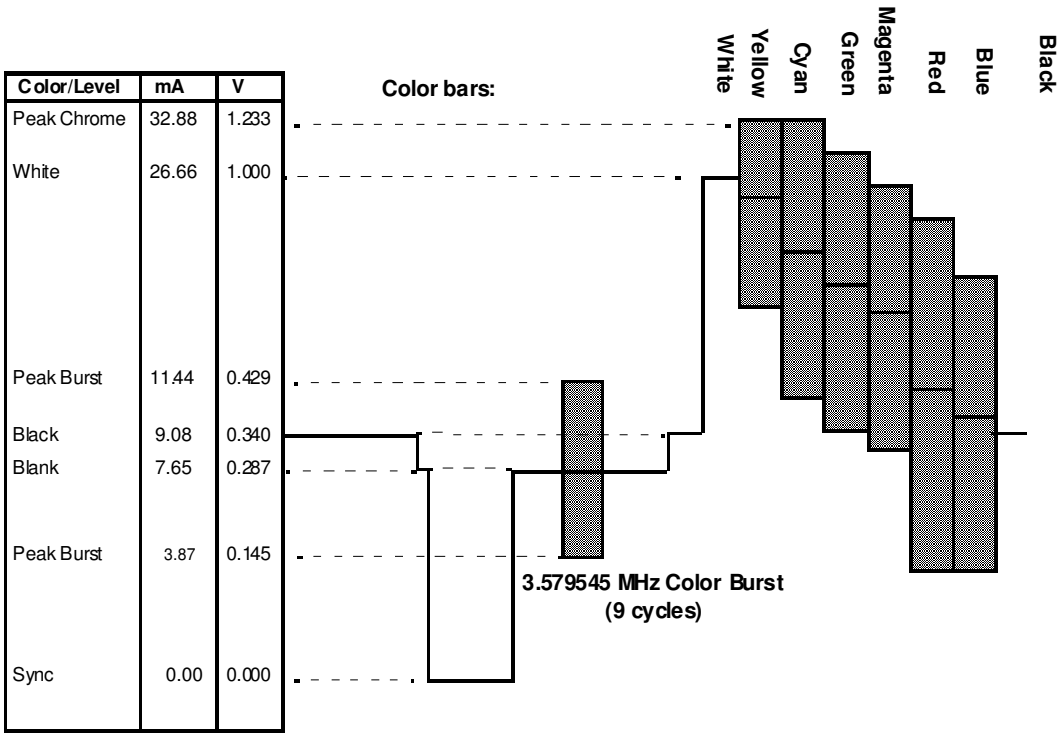

Figure 13: Composite NTSC Video Output Waveform (DACG = 0)

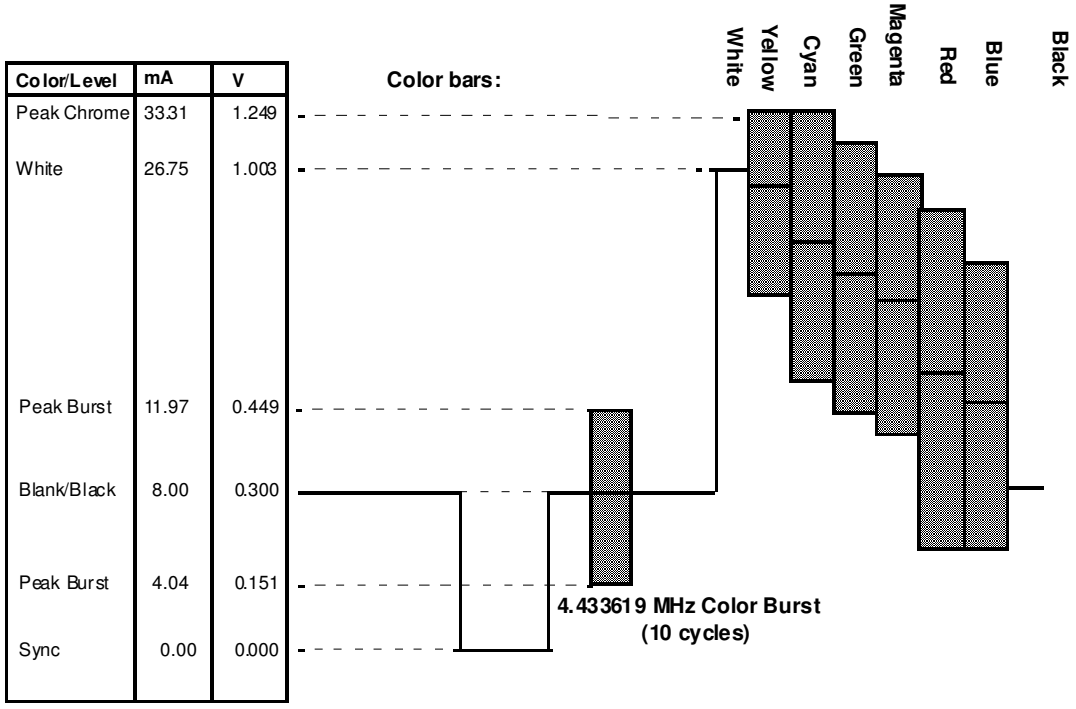

Figure 14: Composite PAL Video Output Waveform (DACG = 1)

2.5 Wide Screen Signaling

WSS algorithms, described by ITU-R.BT.1119 and EIAJ CPR-1204, are used to instruct 16:9 TVs how to display 4:3 programs. Four WSS modes are supported by the CH7016A. See the description for registers 31h – 33h for more details.

2.6 Median Filter

The CH7016A integrates a median filter in de-interlace mode. Instead of outputting an output line that is the simple average between two input lines the median filter analyses several pixels on adjacent lines and outputs the median of the pixel values. This results in reduced blurring in some situations.

The accuracy of the comparison of the pixel values can be controlled using the CMPLMT bit (bit 2 of Register 35h). The median filter can be enabled using the MEDFEN bit (bit 0 of Register 35h).

3.0 REGISTER CONTROL

The CH7016A is controlled via a serial control port. The serial bus uses only the SPC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device should retain all register values during power down modes.

Regarding the CH7016A register read/write operations, please see Application Note AN-61 for details.

3.1 Control Registers Index

The controls are listed below, divided into three sections: General & Power Down controls, Input/Output controls, TV-Out controls.

Table 16: Control Register Index

Name	Description	Address
GENERAL & POWER DOWN CONTROLS		
DACPD[3:0]	DAC Power Down	49h
DID[7:0]	Device ID Register	4Bh
ResetIB	Software SPP (serial port) reset	48h
ResetDB	Software datapath reset	48h
TVPD	TV power down	49h
VID[7:0]	Version ID Register	4Ah
INPUT/OUTPUT CONTROLS		
BCO[2:0]	Select output signal for BCO pin	22h
BCOEN	Enable BCO Output	22h
BCOP	BCO polarity	22h
BGBST	Bandgap Boost	14h
DACBP	DAC bypass	21h
DACG[1:0]	DAC gain control	21h
DACS[1:0]	DAC Switch	08h
DACT[3:0]	DAC termination sense	20h
DES	Decode embedded sync	1Fh
GOENB[1:0]	Direction control for GPIO pins	1Eh
GPHSS	General Purpose / Horizontal Sync Select	48h
GPIOL[1:0]	Read or Write Data for GPIO pins	1Eh
HSP	H sync polarity control	1Fh
IBS	Input buffer type select for D[11:0]	1Fh
IDF[2:0]	Input Data Format for D[11:0]	1Fh, 21h
MCP	XCLK Polarity Control for D[11:0]	1Ch
PCM	P-Out 1X, 2X select	1Ch
POUTE	P-Out enable	1Eh
POUTP	P-Out clock polarity	1Eh
SENSE	TV Sense	20h
SICN	Serial Port N Enable	10h
SICP	Serial Port P Enable	10h
SYNCO[1:0]	Select Sync output on GPIO1	21h
SYO	H/V sync direction control	1Fh
VSP	V sync polarity control for	1Fh
XCM	XCLK 1X / 2X select for D[11:0]	1Ch
XCMD[3:0]	Delay adjust between XCLK and D[11:0]	1Dh
XOSC[2:0]	Crystal oscillator adjustments	21h, 20h

TV-OUT CONTROLS		
BL[7:0]	TV-Out Black level control	07h
BLKEN	Black Level control register update	1Dh
CBW	Chroma video bandwidth	02h
CE[2:0]	TV-Out contrast enhancement	08h
CFF[1:0]	Chroma flicker filter setting	01h
CFRB	Chroma sub-carrier free run (bar) control	02h
CIV[25:0]	Calculated sub-carrier increment value read out	10h-13h
CIVC[1:0]	Calculated sub-carrier control (hysteresis)	10h
CIVEN	Calculated sub-carrier enable	10h
CMPLMT	Median filter comparison limit	08h
CVBWB	CVBS DAC receives black & white (S-Video) signal	02h
EXVBI	Extend vertical blanking interval	47h
FSCI[31:0]	Sub-carrier generation increment value (when CIVEN=0)	0Ch-0Fh
HDTV	Enable HDTV modes	14h
HP[8:0]	TV-Out horizontal position control	05h, 03h
IQEN	Interlaced Quality Enhancement	55h
IR[2:0]	Input data resolution	00h
M/S*	TV-Out PLL reference input control	1Ch
M[8:0]	TV-Out PLL M divider	0Ah, 09h
MEDFEN	Enable median filter	08h
MEM[2:0]	Memory sense amp reference adjust	09h
N[9:0]	TV-Out PLL N divider	0Bh, 09h
$PALN_C$	Select PAL-N (Argentina) when in a CIV mode	10h
PEDL[7:0]	Pedestal level register	4Fh
PLLCAP	TV-Out PLL Capacitor Control	09h
PLLCPI	TV-Out PLL Charge Pump control settings	09h
SAV[8:0]	Horizontal start of active video	04h, 03h
SR[2:0]	TV-Out scaling ratio	00h
TE[2:0]	Text enhancement	03h
VBID	Vertical blanking interval defeat	02h
VOF[1:0]	TV-Out video format (s-video & composite, YPrPb or RGB)	01h
VOS[1:0]	TV-Out video standard	00h
VP[8:0]	TV-Out vertical position control	06h, 03h
YCV[1:0]	Composite video luma bandwidth	02h
YFFH[1:0]	Luma text enhancement flicker filter setting	01h
YFFL[1:0]	Luma flicker filter setting	01h
YSV[1:0]	S-Video luma bandwidth	02h
WSSD[19:0]	Wide Screen Signaling Data	4Ch-4Eh
WSSEN	Wide Screen Signaling Enable	4Eh
WSSS[1:0]	Wide Screen Signaling Format	4Eh
WSSUVF	Enable WSS sine pulse through the UV filter	4Eh

3.2 Control Registers Map

Table 17: Serial Port Register Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	IR2	IR1	IR0	VOS1	VOS0	SR2	SR1	SR0
01h	VOF1	VOF0	CFF1	CFF0	YFFH1	YFFH0	YFFL1	YFFL0
02h	VBID	CFRB	CVBWB	CBW	YSV1	YSV0	YCV1	YCV0
03h	Reserved	Reserved	SAV8	HP8	VP8	TE2	TE1	TE0
04h	SAV7	SAV6	SAV5	SAV4	SAV3	SAV2	SAV1	SAV0
05h	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
06h	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
07h	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
08h	Reserved	DACS1	DACS0	CMPLMT	MEDFEN	CE2	CE1	CE0
09h	MEM2	MEM1	MEM0	N9	N8	M8	PLLCPI	PLLCAP
0Ah	M7	M6	M5	M4	M3	M2	M1	M0
0Bh	N7	N6	N5	N4	N3	N2	N1	N0
0Ch	FSCI31	FSCI30	FSCI29	FSCI28	FSCI27	FSCI26	FSCI25	FSCI24
0Dh	FSCI23	FSCI22	FSCI21	FSCI20	FSCI19	FSCI18	FSCI17	FSCI16
0Eh	FSCI15	FSCI14	FSCI13	FSCI12	FSCI11	FSCI10	FSCI9	FSCI8
0Fh	FSCI7	FSCI6	FSCI5	FSCI4	FSCI3	FSCI2	FSCI1	FSCI0
10h	SICP	SICN	CIV25	CIV24	CIVC1	CIVC0	$PALN_C$	CIVEN
11h	CIV23	CIV22	CIV21	CIV20	CIV19	CIV18	CIV17	CIV16
12h	CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8
13h	CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0
14h	BGBST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HDTV
1Ch	Reserved	Reserved	Reserved	Reserved	M/S*	MCP	PCM	XCM
1Dh	Reserved	BLKEN	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
1Eh	GOENB1	GOENB0	GPIOL1	GPIOL0	Reserved	Reserved	POUTE	POUTP
1Fh	IBS	DES	SYO	VSP	HSP	IDF2	IDF1	IDF0
20h	Reserved	XOSC2	Reserved	DACT3	DACT2	DACT1	DACT0	SENSE
21h	XOSC1	XOSC0	Reserved	SYNCO1	SYNCO0	DACG1	DACG0	DACBP
22h	SHF2	SHF1	SHF0	BCOEN	BCOP	BCO2	BCO1	BCO0
48h	GPHSS	Reserved	Reserved	ResetIB	ResetDB	Reserved	Reserved	Reserved
49h	Reserved	Reserved	Reserved	DACPD3	DACPD2	DACPD1	DACPD0	TVPD
4Ah	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
4Bh	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
4Ch	WSSD7	WSSD6	WSSD5	WSSD4	WSSD3	WSSD2	WSSD1	WSSD0
4Dh	WSSD15	WSSD14	WSSD13	WSSD12	WSSD11	WSSD10	WSSD9	WSSD8
4Eh	WSSEN	WSSUVF	WSSS1	WSSS0	WSSD19	WSSD18	WSSD17	WSSD16
4Fh	PEDL7	PEDL6	PEDL5	PEDL4	PEDL3	PEDL2	PEDL1	PEDL0
55h	IQEN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

3.3 Control Registers Description

Display Mode Register

Symbol: **DM**
Address: **00h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	IR2	IR1	IR0	VOS1	VOS0	SR2	SR1	SR0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	0	1	0	1	0

Register DM provides programmable control of the CH7016A TV display modes, including input resolution (IR[2:0]), video output standard (VOS[1:0]), and scaling ratio (SR[2:0]). The mode of operation is determined according to **Table 18** below when the HDTV bit (Register 14h, bit 0) = '1'. These are the HDTV modes. When HDTV bit (Register 03h, bit 7) = '0' the mode of operation is determined according to **Table 19**. These are the SDTV modes. For entries in which the output standard is shown as PAL, PAL-B, D, G, H, I, N_C can be supported through proper selection of the chroma sub-carrier. For entries in which the output standard is shown as NTSC, NTSC-M,J and PAL-M can be supported through proper selection of VOS[1:0] and chroma sub-carrier.

Table 18: Display Mode for HDTV/Component TV (HDTV = '1')

Mode	IR[2:0]	VOS [1:0]	SR [2:0]	Input Data Format (Active Video)	Total Pixels/Line x Total Lines/Frame	Output Standard [TV Standard]	Frame Rate [Hz]	Pixel Clock [MHz]
48	000	00	000	720x480	858x525	EIA-770.2-A	60	27.027
49	001	00	000	720x483	858x525	SMPTE293M	60/1.001	27.0
50	000	10	001	1280x720	1650x750	SMPTE296M	60	74.250
51	000	01	001	1920x1080	2376x1250	SMPTE295M	25	74.250
52	001	10	100	1920x1080	2376x1250	SMPTE295M	50	148.500
53	001	01	001	1920x1080	2200x1125	SMPTE274M	30	74.250
54	010	01	001	1920x1080	2640x1125	SMPTE274M	25	74.250
55	010	10	100	1920x1080	2200x1125	SMPTE274M	60	148.500
56	011	10	100	1920x1080	2640x1125	SMPTE274M	50	148.500
57	100	10	001	1920x1080	2200x1125	SMPTE274M	30	74.250
58	101	10	001	1920x1080	2750x1125	SMPTE274M	24	74.250
59	110	10	001	1920x1080	2640x1125	SMPTE274M	25	74.250
60	010	00	000	720x576	864x625	ITU-R BT.1358	50	27.000
61 [1]	000	11	000	720x480	858x525	ITU-R BT.1358 / EIA-770.1-A	30	13.500
62 [1]	001	11	000	720x576	864x625	ITU-R BT.1358	25	13.500
63	000	00	010	720x480	856x525		60	26.937
64	001	00	010	720x483	856x525		60	26.964
65	000	10	011	1280x720	1648x750		60	74.160
66	101	10	011	1920x1080	2752x1125		24	74.304

[1] These modes operate with interlaced input and progressive output.

Table 19: Display Mode for Standard TV (HDTV = '0')

Mode	IR[2:0]	VOS [1:0]	SR[2:0]	Input Data Format (Active Video)	Total Pixels/Line x Total Lines/Frame	Output Standard [TV Standard]	Scaling	Percent Overscan	Pixel Clock (MHz)
0	000	00	000	512x384	840x500	PAL	5/4	-17	21.000000
1	000	00	001	512x384	840x625	PAL	1/1	-33	26.250000
2	000	01	000	512x384	800x420	NTSC	5/4	0	20.139860
3	000	01	001	512x384	784x525	NTSC	1/1	-20	24.671329
4	001	00	000	720x400	1125x500	PAL	5/4	-13	28.125000
5	001	00	001	720x400	1152x625	PAL	1/1	-30	36.000000
6	001	01	000	720x400	945x420	NTSC	5/4	+4	23.790210
7	001	01	001	720x400	936x525	NTSC	1/1	-16	29.454545
8	010	00	000	640x400	1000x500	PAL	5/4	-13	25.000000
9	010	00	001	640x400	1008x625	PAL	1/1	-30	31.500000
10	010	01	000	640x400	840x420	NTSC	5/4	+4	21.146854
11	010	01	001	640x400	832x525	NTSC	1/1	-17	26.181819
12	010	01	010	640x400	840x600	NTSC	7/8	-27	30.209791
13	011	00	000	640x480	840x500	PAL	5/4	+4	21.000000
14	011	00	001	640x480	840x625	PAL	1/1	-17	26.250000
15	011	00	011	640x480	840x750	PAL	5/6	-30	31.500000
16	011	01	001	640x480	784x525	NTSC	1/1	0	24.671329
17	011	01	010	640x480	784x600	NTSC	7/8	-13	28.195805
18	011	01	011	640x480	800x630	NTSC	5/6	-18	30.209790
19	100	01	001	720x480	882x525	NTSC	1/1	0	27.755245
20	100	01	010	720x480	882x600	NTSC	7/8	-13	31.720280
21	100	01	011	720x480	900x630	NTSC	5/6	-18	33.986015
22	101	00	001	720x576	882x625	PAL	1/1	0	27.562500
23	101	00	011	720x576	900x750	PAL	5/6	-18	33.750000
24	101	00	100	720x576	900x875	PAL	5/7	-30	39.375000
25	110	00	001	800x600	944x625	PAL	1/1	+4	29.500000
26	110	00	011	800x600	960x750	PAL	5/6	-14	36.000000
27	110	00	100	800x600	960x875	PAL	5/7	-27	42.000000
28	110	01	110	800x600	1040x700	NTSC	¾	-6	43.636364
29	110	01	111	800x600	1064x750	NTSC	7/10	-14	47.832169
30	110	01	101	800x600	1040x840	NTSC	5/8	-22	52.363637
31	111	00	100	1024x768	1400x875	PAL	5/7	-4	61.250000
32	111	00	101	1024x768	1400x1000	PAL	5/8	-16	70.000000
33	111	00	110	1024x768	1400x1125	PAL	5/9	-25	78.750000
34	111	01	101	1024x768	1160x840	NTSC	5/8	0	58.405595
35	111	01	110	1024x768	1160x945	NTSC	5/9	-10	65.706295
36	111	01	111	1024x768	1168x1050	NTSC	1 / 2	-20	73.510491
37 [2]	101	00	000	720x576	864x625	PAL	1/1	0	13.500000
38 [2]	100	01	000	720x480	858x525	NTSC	1/1	0	13.500000
39	001	01	111	720x400	900x441	NTSC	25/21	-1	23.790210
40	010	01	111	640x400	800x441	NTSC	25/21	-1	21.146854
41	011	00	111	640x480	800x525	PAL	25/21	-1	21.000000
42	100	01	101	720x480	880x525	NTSC	1/1	0	27.692308
43	100	01	110	720x480	784x600	NTSC	7/8	-13	28.195805
44	100	01	111	720x480	880x630	NTSC	5/6	-18	33.230770
45	101	00	101	720x576	888x625	PAL	1/1	0	27.750000
46	101	00	110	720x576	880x750	PAL	5/6	-18	33.000000
47	101	00	111	720x576	880x875	PAL	5/7	-30	38.500000

[2] These DVD modes operate with interlaced input. Scan conversion and flicker filter are bypassed.

Table 20: Video Output Standard Selection

VOS[1:0]	00	01	10	11
Output Format	PAL	NTSC	PAL-M	NTSC-J

Output Format Register

Symbol: **OF**
Address: **01h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VOF1	VOF0	CFF1	CFF0	YFFH1	YFFH0	YFFL1	YFFL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	0	0	1	1	1

YFFL[1:0] (bits 1-0) of Register FF control the filter used in the scaling and flicker reduction block applied to the non-text portion (low frequency) of the luminance signal as shown in the table below.

YFFH[1:0] (bits 3-2) of Register FF control the filter used in the scaling and flicker reduction block applied to the text portion (high frequency) of the luminance signal as shown in the table below.

Table 21: Luma Flicker Filter Control

	YFFH and YFFL Flicker Filter Settings (lines)			
Scaling Ratio	**00**	**01**	**10**	**11**
5/4	2	3	3	3
1/1, 7/8, 5/6, 3/4, 5/7, 7/10	2	3	4	5
5/8	2	3	4	6
25/21	2	3	6	6
5/9	3	4	5	6
½	3	5	5	7

CFF[1:0] (bits 5-4) of Register FF control the filter used in the scaling and flicker reduction block applied to the chrominance signal as shown in **Table 21** below. A setting of '11' applies a dot crawl reduction filter which can reduce the 'hanging dots' effect of an NTSC composite video signal when displayed on a TV with a comb filter.

Table 22: Chroma Flicker Filter Control

	CFF Flicker Filter Settings (lines)			
Scaling Ratio	**00**	**01**	**10**	**11**
5/4	2	3	3	3
1/1, 7/8, 5/6, 3/4, 5/7, 7/10	2	3	4	5
5/8	2	3	4	5
25/21	2	3	4	6
5/9	3	4	5	6
½	3	5	5	7

VOF[1:0] (bits 7-6) of Register FF control the video output format. Must be set per the table below:

Table 23: TV Output Configurations

VOF1	VOF0	TV Output Configuration
0	0	YCrCb
0	1	Composite, S-Video
1	0	YPrPb
1	1	SCART + Composite

For the TV out DAC by-pass for RGB out, refer to DACBP (bit0 of Register 21h). Refer to **Table 9** in section 2.2 for TV Output DAC configurations. Y, Cr and Cb are output on the same DACs as Y, Pr and Pb respectively.

Video Bandwidth Register

Symbol: **VBW**
Address: **02h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VBID	CFRB	CVBWB	CBW	YSV1	YSV0	YCV1	YCV0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	1	1	1	1	0

YCV[1:0] (bits 1-0) of Register VBW control the filter used to limit the bandwidth of the luma signal in the CVBS output signal. A table of –3dB bandwidth values is given in **Table 24** below.

YSV[1:0] (bits 3-2) of Register VBW control the filter used to limit the bandwidth of the luma signal in the S-Video output signal. A table of –3dB bandwidth values is given in **Table 24** below.

CBW (bit 4) of Register VBW controls the filter used to limit the bandwidth of the chroma signal in the CVBS and S-Video output signals. A table of –3dB bandwidth values is given in **Table 24** below.

Note that modes 48 to 62 are all for HDTV application so data for these modes does not go through the CBW, YSV or YCV bandwidth limited filters.

Table 24: Video Bandwidth

Mode	CBW		YSV[1:0] and YCV[1:0]			
	0	1	00	01	10	11
0	0.620	0.856	2.300	2.690	3.540	5.880
1	0.775	1.070	2.880	3.360	4.430	7.350
2	0.529	0.730	1.960	2.290	3.020	5.010
3	0.648	0.894	2.410	2.810	3.700	6.140
4	0.831	1.150	3.080	3.600	4.750	7.870
5	1.060	1.470	3.950	4.610	6.080	10.100
6	0.703	0.970	2.610	3.040	4.010	6.660
7	0.870	1.200	3.230	3.770	4.970	8.240
8	0.738	1.020	2.740	3.200	4.220	7.000
9	0.930	1.280	3.460	4.030	5.320	8.820
10	0.624	0.862	2.320	2.710	3.570	5.920
11	0.773	1.070	2.870	3.350	4.420	7.330
12	0.892	1.230	3.310	3.870	5.100	8.450
13	0.620	0.856	2.300	2.690	3.540	5.880
14	0.775	1.070	2.880	3.360	4.430	7.350
15	0.930	1.280	3.460	4.030	5.320	8.820
16	0.648	0.894	2.410	2.810	3.700	6.140
17	0.740	1.020	2.750	3.210	4.230	7.010
18	0.793	1.100	2.950	3.440	4.530	7.510
19	0.729	1.010	2.710	3.160	4.160	6.900
20	0.833	1.150	3.090	3.610	4.760	7.890
21	0.892	1.230	3.310	3.870	5.100	8.450
22	0.724	0.999	2.690	3.140	4.130	6.860
23	0.886	1.220	3.290	3.840	5.060	8.400
24	1.030	1.430	3.840	4.480	5.910	9.790
25	0.774	1.070	2.880	3.360	4.430	7.340
26	0.945	1.310	3.510	4.100	5.400	8.960
27	1.100	1.520	4.100	4.780	6.300	10.400
28	0.859	1.190	3.190	3.720	4.910	8.140
29	0.942	1.300	3.500	4.080	5.380	8.920
30	1.030	1.420	3.830	4.470	5.890	9.770
31	0.804	1.110	2.990	3.480	4.590	7.620
32	0.919	1.270	3.410	3.980	5.250	8.710
33	1.030	1.430	3.840	4.480	5.910	9.790
34	0.767	1.060	2.850	3.320	4.380	7.260
35	0.862	1.190	3.200	3.740	4.930	8.170
36	0.965	1.330	3.580	4.180	5.510	9.140
37	0.709	0.979	2.630	3.070	4.050	6.720
38	0.466	0.643	1.730	2.020	2.660	4.410
39	0.703	0.970	2.610	3.040	4.010	6.660
40	0.624	0.862	2.320	2.710	3.570	5.920
41	0.620	0.856	2.300	2.690	3.540	5.880
42	0.727	1.003	2.696	3.153	4.149	6.892
43	0.833	1.150	3.090	3.610	4.760	7.890
44	0.892	1.231	3.309	3.870	5.093	8.459
45	0.728	1.005	2.702	3.160	4.158	6.907
46	0.866	1.196	3.213	3.757	4.945	8.213
47	1.010	1.395	3.748	4.384	5.769	9.582

CVBWB (bit 5) of Register VBW controls the chroma component of the CVBS signal. CVBWB = '0' disables the chroma signal being added to the CVBS signal so the output on the CVBS pin is S-video luminance, CVBWB = '1' enables the chroma signal being added to the CVBS signal. Setting CVBWB = '0' enables the output of a black and

white image on the composite output, thereby eliminating the degrading effects of the color signal (such as dot crawl and false colors). This is useful for viewing text with high accuracy. This also allows the output of either S-video or CVBS using just 2 DACs which is useful in situations where connector space is at a premium.

CFRB (bit 6) of Register VBW controls whether the chroma sub-carrier free-runs, or is locked to the video signal. A '1' causes the sub-carrier to lock to the TV vertical rate, and should be used when the CIVEN bit (Register 10h) is set to '0'. A '0' causes the sub-carrier to free-run, and should be used when the CIVEN bit is set to '1'.

VBID (bit 7) of Register VBW controls the vertical blanking interval defeat function. A '1' in this register location forces the flicker filter to minimum filtering during the vertical blanking interval. A '0' in this location causes the flicker filter to remain at the same setting inside and outside of the vertical blanking interval.

Text Enhancement Register

Symbol: **TE**
Address: **03h**
Bits: **6**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	SAV8	HP8	VP8	TE2	TE1	TE0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	1	0	1

TE[2:0] (bits 2-0) of Register TE control the text enhancement circuitry within the CH7016A. A value of '000' minimizes the enhancement feature, while a value of '111' maximizes the enhancement.

SAV8, HP8 and VP8 (bits 5-3) of Register TE contain the MSB values for the start of active video, horizontal position and vertical position controls. They are described in detail in the SAV (address 04h), HP (address 05h) and VP (address 06h) register descriptions.

Start of Active Video Register

Symbol: **SAV**
Address: **04h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SAV7	SAV6	SAV5	SAV4	SAV3	SAV2	SAV1	SAV0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	1	0	0	0	0

Register SAV controls the delay, in pixel increments, from leading edge of horizontal sync to start of active video. The entire bit field SAV[8:0] is comprised of this Register SAV[7:0], plus SAV[8] contained in the Text Enhancement Register (03h, bit 5). This is decoded as a whole number of pixels, which can be set anywhere between 0 and 511 pixels. Therefore, in any 2X clock mode the number of 2X clocks from the leading edge of Hsync to the first active data must be a multiple of two clocks.

Horizontal Position Register

Symbol: HP
Address: 05h
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	1	0	0	0	0

Register HP is used to shift the displayed TV image in a horizontal direction (left or right) to achieve a horizontally centered image on screen. The entire bit field, HP[8:0], is comprised of this Register HP[7:0] plus HP[8] contained in the Text Enhancement register (03h, bit 4). For SDTV, increasing values move the displayed image position right, and decreasing values move the image position left. For HDTV, increasing values move the displayed image position left, and decreasing values move the image position right. Horizontal positioning is not available in modes 37 and 38.

Note: The HP Register should not be set to 0.

Vertical Position Register

Symbol: VP
Address: 06h
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Register VP is used to shift the displayed TV image in a vertical direction (up or down) to achieve a vertically centered image on screen. The entire bit field, VP[8:0], is comprised of this Register VP[7:0] plus VP[8] contained in the Text Enhancement Register (03h, bit 3). The value represents the TV line number (relative to the VGA vertical sync) used to initiate the generation and insertion of the TV vertical interval (i.e. the first sequence of equalizing pulses). Increasing values delay the output of the TV vertical sync, causing the image position to move up on the TV screen. Decreasing values, therefore, move the image position DOWN. Each increment moves the image position by one TV line (approximately 2 input lines). The maximum value that should be programmed into VP[8:0] is the number of TV lines per field minus one half (262 or 312). When panning the image up, the number should be increased until (TVLPF-1/2) is reached, the next step should be to reset the register to zero. When panning the image down the screen, decrement the VP[8:0] value until the value zero is reached. The next step should set the register to TVLPF-1/2, and then decrement for further changes.

Note for software: The VP Register must be set to a number > 0.

Black Level Register

Symbol: **BL**
Address: **07h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	1	1

Register BL controls the black level. This allows control of the brightness independent of the pedestal level (see the description for Register 4Fh). The luminance data is added to this black level, which must be set between 65 and 170. The default values for the black level are the same as the pedestal. When the input data format is 0 through 3 these values are 131 for NTSC and PAL-M with DACG[1:0] (Register 21h) = '00', 109 for PAL with DACG[1:0] = '01' and 102 for NTSC-J with DACG[1:0] = '01'. When the input data format is 4 the default values are 112 for NTSC and PAL-M with DACG[1:0] = '10', 94 for PAL with DACG[1:0] = '11'and 88 for NTSC-J and SDTV YPrPb with DACG[1:0] = '11'. The default value is always 117 for HDTV YPrPb. The suggested BL setting for HDTV is between 117 and 170 with DACG[1:0] (Register 21h, bits 2-1) = '01' and BGBST (Register 14h, bit 7) = '1'. See also the description for the BLKEN bit (Register 1Dh, bit 6).

Contrast Enhancement Register

Symbol: **CE**
Address: **08h**
Bits: **7**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	DACS1	DACS0	CMPLMT	MEDFEN	CE2	CE1	CE0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	1	1

CE[2:0] (bits 2-0) of Register CE control the contrast enhancement feature of the CH7016A, according to **Figure 15**. A setting of '0' results in reduced contrast, a setting of '1' leaves the image contrast unchanged, and values beyond '1' result in increased contrast. [Note: The straight line denotes Yout = Yin and therefore no enhancement.]

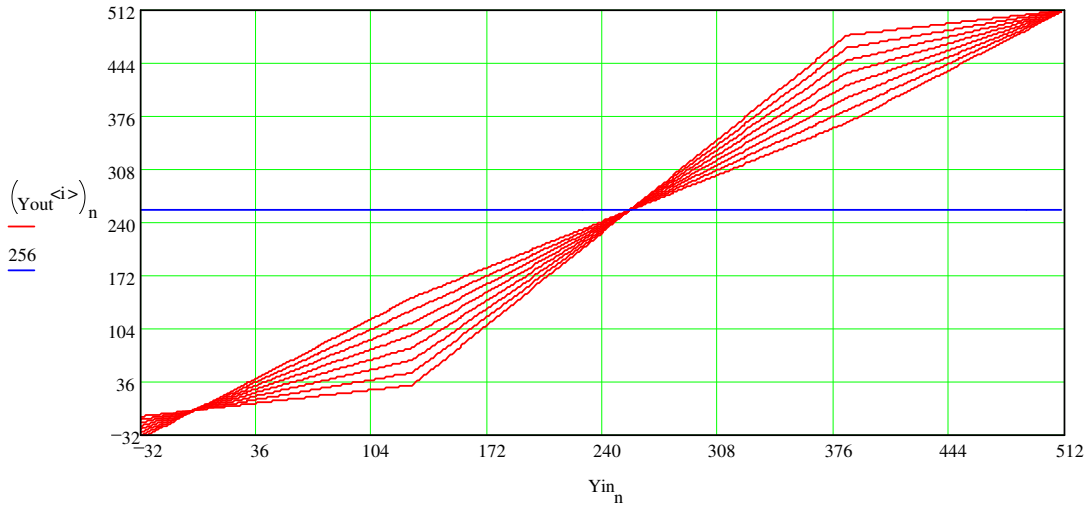

Figure 15: Contrast Enhancement of the CH7016A

MEDFEN (bit 3) of Register CE enables the median filter.

MEDFEN = 0 => Median filter disabled
= 1 => Median filter enabled

CMPLMT (bit 4) of Register CE controls the number of significant bits of a pixel value to compare in the median filter.

CMPLMT = 0 => Use 8 bit comparison
= 1 => Use 5 bit comparison

DACS[1:0] (bits 6-5) of Register CE control the TV DAC (DACA and DACB) analog switch per the following table. Refer also to **Table 9**.

Table 25: TV DAC Analog Switch Control

DACS1	DACS0	DACA path	DACB path
0	0	Off	Off
0	1	Off	On
1	0	On	Off
1	1	On	On

TV PLL Control Register

Symbol: **TPC**
Address: **09h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	MEM2	MEM1	MEM0	N9	N8	M8	PLLCPI	PLLCAP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

PLLCAP (bit 0) of Register TPC controls the TV PLL loop filter capacitor. A recommended listing of PLLCAP settings versus mode is given in **Table 26**.

Table 26: PLLCAP setting vs. Display Mode

Mode	PLLCAP Value	Mode	PLLCAP Value	Mode	PLLCAP Value
0	1	24	1	48	1
1	1	25	0	49	0
2	0	26	1	50	1
3	0	27	1	51	0
4	1	28	1	52	1
5	1	29	0	53	0
6	0	30	1	54	0
7	1	31	1	55	1
8	0	32	1	56	1
9	1	33	1	57	0
10	0	34	0	58	0
11	1	35	0	59	0
12	0	36	0	60	1
13	1	37	1	61	1
14	1	38	1	62	1
15	1	39	0	63	1
16	0	40	0	64	0
17	0	41	1	65	1
18	0	42	0	66	0
19	0	43	0		
20	0	44	0		
21	0	45	0		
22	1	46	0		
23	1	47	1		

PLLCPI (bit 1) of Register TPC should be left at the default value.

M8 and N[9:8] (bits 4-2) of Register TPC contain the MSB values for the TV PLL divider ratio's. These controls are described in detail in the PLLM (address 0Ah) and PLLN (address 0Bh) register descriptions.

MEM[0] (bit 5) of Register TPC controls the input latch bias current level. The default value is recommended.

MEM[2:1] (bits 7-6) of Register TPC control the memory sense amp reference level. The default value is recommended.

TV PLL M Value Register

Symbol: **PLLM**
Address: **0Ah**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	M7	M6	M5	M4	M3	M2	M1	M0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	1	1	1	1	1

Register PLLM controls the division factor applied to the 14.31818MHz frequency reference clock before it is input to the TV PLL phase detector when the CH7016A is operating in clock master mode. The entire bit field, M[8:0], is comprised of this Register M[7:0] plus M[8] contained in the TV PLL Control Register (09h, bit2). In slave mode, an external pixel clock is used instead of the 14.31818MHz frequency reference, but the division factor is also controlled by M[8:0]. In slave mode, the value of 'M' is internally set to 1. Tables of values versus display mode are given following the PLLN Register description.

TV PLL N Value Register

Symbol: **PLLN**
Address: **0Bh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N7	N6	N5	N4	N3	N2	N1	N0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	1	1	1	1	0

Register PLLN controls the division factor applied to the VCO output before being applied to the PLL phase detector, when the CH7016A is operating in clock master mode. The entire bit field, N[9:0], is comprised of this Register N[7:0] plus N[9:8] contained in the TV PLL Control Register (09h, bits 3 and 4). In slave mode, the value of 'N' is internally set to 1. The pixel clock generated in clock master modes is calculated according to the equation Fpixel = Fref * [(N+2) / (M+2)]. When using a 14.31818MHz frequency reference, the required M and N values for each mode are shown in the following tables:

Table 27: TV PLL M and N values vs. Display Mode

Mode	VGA Resolution, TV Standard, Scaling Ratio	N 10-bits (dec)	N 10-bits (hex)	M 9-bits (dec)	M 9-bits (hex)
0	512x384, PAL, 5:4	20	0x14	13	0x0D
1	512x384, PAL, 1:1	9	0x09	4	0x04
2	512x384, NTSC, 5:4	126	0x7E	89	0x59
3	512x384, NTSC, 1:1	110	0x6E	63	0x3F
4	720x400, PAL, 5:4	53	0x35	26	0x1A
5	720x400, PAL, 1:1	86	0x56	33	0x21
6	720x400, NTSC, 5:4	106	0x6A	63	0x3F
7	720x400, NTSC, 1:1	70	0x46	33	0x21
8	640x400, PAL, 5:4	108	0x6C	61	0x3D
9	640x400, PAL, 1:1	9	0x09	3	0x03
10	640x400, NTSC, 5:4	94	0x5E	63	0x3F
11	640x400, NTSC, 1:1	62	0x3E	33	0x21
12	640x400, NTSC, 7:8	190	0xBE	89	0x59
13	640x480, PAL, 5:4	20	0x14	13	0x0D
14	640x480, PAL, 1:1	9	0x09	4	0x04
15	640x480, PAL, 5:6	9	0x09	3	0x03
16	640x480, NTSC, 1:1	110	0x6E	63	0x3F
17	640x480, NTSC, 7:8	126	0x7E	63	0x3F
18	640x480, NTSC, 5:6	190	0xBE	89	0x59
19	720x480, NTSC, 1:1	124	0x7C	63	0x3F
20	720x480, NTSC, 7:8	142	0x8E	63	0x3F
21	720x480, NTSC, 5:6	214	0xD6	89	0x59
22	720x480, PAL, 1:1	75	0x4B	38	0x26
23	720x480, PAL, 5:6	31	0x1F	12	0x0C
24	720x480, PAL, 5:7	9	0x09	2	0x02
25	800x600, PAL, 1:1	647	0x287	313	0x139
26	800x600, PAL, 5:6	86	0x56	33	0x21
27	800x600, PAL, 5:7	42	0x2A	13	0x0D
28	800x600, NTSC, 3:4	62	0x3E	19	0x13
29	800x600, NTSC, 7:10	302	0x12E	89	0x59
30	800x600, NTSC, 5/8	126	0x7E	33	0x21
31	1024x768, PAL, 5:7	75	0x4B	16	0x10
32	1024x768, PAL, 5:8	42	0x2A	7	0x07
33	1024x768, PAL, 5:9	20	0x14	2	0x02
34	1024x768, NTSC, 5:8	565	0x235	137	0x89
35	1024x768, NTSC, 5:9	333	0x14D	71	0x47
36	1024x768, NTSC, 1:2	917	0x395	177	0xB1
37	720x576, PAL, 1:1	31	0x1F	33	0x21
38	720x480, NTSC, 1:1	31	0x1F	33	0x21
39	720x480, NTSC, 1:1	106	0x6A	63	0x3F
40	640x400, NTSC, 25:21	94	0x5E	63	0x3F
41	640x480, PAL,25:21	20	0x14	13	0x0D
42	720x480, NTSC, 1:1	174	0xAE	89	0x59
43	720x480, NTSC, 7:8	126	0x7E	63	0x3F
44	720x480, NTSC, 5:6	309	0x135	132	0x84
45	720x576, PAL, 1:1	405	0x195	208	0xD0
46	720x576, PAL, 5:6	240	0xF0	103	0x67
47	720x576, PAL, 5:7	119	0x77	43	0x2B

Table 28: HDTV PLL M and N values vs. Display Mode

Mode	Input Resolution, TV Standard	N 10-bits (dec)	N 10-bits (hex)	M 9-bits (dec)	M 9-bits (hex)
48	720x480, EIA-770.2-A	485	0x1E5	256	0x100
49	720x483, SMPTE293M	64	0x40	33	0x21
50	1280x720, SMPTE296M	361	0x169	68	0x44
51	1920x1080, SMPTE295M	361	0x169	68	0x44
52	1920x1080, SMPTE295M	361	0x169	33	0x21
53	1920x1080, SMPTE274M	361	0x169	68	0x44
54	1920x1080, SMPTE274M	361	0x169	68	0x44
55	1920x1080, SMPTE274M	361	0x169	33	0x21
56	1920x1080, SMPTE274M	361	0x169	33	0x21
57	1920x1080, SMPTE274M	361	0x169	68	0x44
58	1920x1080, SMPTE274M	361	0x169	68	0x44
59	1920x1080, SMPTE274M	361	0x169	68	0x44
60	720x576, ITU-R BT.1358	64	0x40	33	0x21
61	720x480, ITU-R BT.1358 / EIA-770.1-A	31	0x1F	33	0x21
62	720x576, ITU-R BT.1358	31	0x1F	33	0x21
63	720x480	743	0x2EF	394	0x18A
64	720x483	917	0x395	486	0x1E6
65	1280x720	200	0xC8	37	0x25
66	2752x1125	491	0x1EB	93	0x5D

Sub-carrier Value Register

Symbol: FSCI
Address: 0Ch –0Fh
Bits: 8 each

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:								

Registers FSCI contain a 32-bit value which is used as an increment value for the ROM address generation circuitry when CIVEN=0. The bit locations are specified as follows:

Register	Contents
0Ch	FSCI[31:24]
0Dh	FSCI[23:16]
0Eh	FSCI[15:8]
0Fh	FSCI[7:0]

When the CH7016A is used in the clock master mode, the following tables should be used to set the FSCI registers. When using these values, the CIVEN bit in Register 10h should be set to ‘0’, and the CFRB bit in Register 02h should be set to ‘1’.

Table 29: FSCI Values (525-Line TV-Out Modes)

Mode	NTSC "Normal Dot Crawl" (dec)	NTSC "Normal Dot Crawl" **(hex)**	NTSC "No Dot Crawl" (dec)	NTSC "No Dot Crawl" **(hex)**	PAL-M "Normal Dot Crawl" (dec)	PAL-M "Normal Dot Crawl" (hex)
2	763,363,328	0x2D800000	763,366,524	0x2D800C7C	762,524,467	0x2D733333
3	623,153,737	0x25249249	623,156,346	0x25249C7A	622,468,953	0x251A1F59
6	574,429,782	0x223D1A56	574,432,187	0x223D23BB	573,798,541	0x2233788D
7	463,962,517	0x1BA78195	463,964,459	0x1BA7892B	463,452,668	0x1B9FB9FC
10	646,233,505	0x2684BDA1	646,236,211	0x2684C833	645,523,358	0x2679E79E
11	521,957,831	0x1F1C71C7	521,960,019	0x1F1C7A53	521,384,251	0x1F13B13B
12	452,363,454	0x1AF684BE	452,365,347	0x1AF68C23	451,866,351	0x1AEEEEEF
16	623,153,737	0x25249249	623,156,346	0x25249C7A	622,468,953	0x251A1F59
17	545,259,520	0x20800000	545,261,803	0x208008EB	544,660,334	0x2076DB6E
18	508,908,885	0x1E555555	508,911,016	0x1E555DA8	508,349,645	0x1E4CCCCD
19	553,914,433	0x21041041	553,916,752	0x21041950	553,305,736	0x20FAC688
20	484,675,129	0x1CE38E39	484,677,158	0x1CE39626	484,142,519	0x1CDB6DB7
21	452,363,454	0x1AF684BE	452,365,347	0x1AF68C23	451,866,351	0x1AEEEEEF
28	469,762,048	0x1C000000	469,764,015	0x1C0007AF	469,245,826	0x1BF81F82
29	428,554,851	0x198B3A63	428,556,645	0x198B4165	428,083,911	0x19840AC7
30	391,468,373	0x17555555	391,470,012	0x17555BBC	391,038,188	0x174EC4EC
34	526,457,468	0x1F611A7C	526,459,671	0x1F612317	525,878,943	0x1F58469F
35	467,962,193	0x1BE48951	467,964,152	0x1BE490F8	467,447,949	0x1BDCB08D
36	418,281,276	0x18EE773C	418,283,027	0x18EE7E13	417,821,626	0x18E773BA
38	569,408,543	0x21F07C1F	569,410,927	0x21F0856F	568,782,819	0x21E6EFE3
39	574,429,782	0x223D1A56	574,432,187	0x223D23BB	573,798,541	0x2233788D
40	646,233,505	0x2684BDA1	646,236,211	0x2684C833	645,523,358	0x2679E79E
42	555,173,329	0x211745D1	555,175,654	0x21174EE6	554,563,249	0x210DF6B1
43	484,675,129	0x1CE38E39	484,677,158	0x1CE39626	484,142,519	0x1CDB6DB7
44	462,644,441	0x1B9364D9	462,646,378	0x1B936C6A	462,136,041	0x1B8BA2E9

Table 30: FSCI Values (625-Line TV-Out Modes)

Mode	PAL "Normal Dot Crawl"	PAL-N (Argentina) "Normal Dot Crawl"
0	806,021,060	651,209,077
1	644,816,848	520,967,262
4	601,829,058	486,236,111
5	470,178,951	379,871,962
8	677,057,690	547,015,625
9	537,347,373	434,139,385
13	806,021,060	651,209,077
14	644,816,848	520,967,262
15	537,347,373	434,139,385
22	690,875,194	558,179,209
23	564,214,742	455,846,354
24	483,612,636	390,725,446
25	645,499,916	521,519,134
26	528,951,320	427,355,957
27	453,386,846	366,305,106
31	621,787,675	502,361,288
32	544,064,215	439,566,127
33	483,612,636	390,725,446
37	705,268,427	569,807,942
41	806,021,060	651,209,077
45	686,207,118	554,407,728
46	577,037,804	466,206,498
47	494,603,832	399,605,570

CIV Control Register

Symbol: CIVC
Address: 10h
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SICP	SICN	CIV25	CIV24	CIVC1	CIVC0	$PALN_C$	CIVEN
TYPE:	R/W	R/W	R	R	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	1

CIVEN (bit 0) of Register CIVC controls whether the FSCI value is used to set the sub-carrier frequency, or the automatically calculated (CIV) value. When the CIVEN value is '1', the number calculated and present at the CIV registers will automatically be used as the increment value for sub-carrier generation. Whenever this bit is set to '1', the CFRB bit should be set to '0'.

$PALN_C$ (bit 1) of Register CIVC forces the CIV algorithm to generate the PAL-N (Argentina) sub-carrier frequency when it is set to '1'. When this bit is set to '0', the VOS[1:0] value is used by the CIV algorithm to determine which sub-carrier frequency to generate.

CIVC[1:0] (bits 3-2) of Register CIVC control the hysteresis circuit which is used to calculate the CIV value. The default value should be used.

CIV[25:24] (bits 5-4) of Register CIVC contain the MSB values for the calculated increment value (CIV) readout. This is described in detail in the CIV (address 11h-13h) register description.

SICP and SICN (bits 7-6) of Register CIVC enable the Serial Port. The default value is recommended.

Calculated Increment Value Register

Symbol: **CIV**
Address: **11h –13h**
Bits: **8 each**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CIV#	CIV#	CIV#	CIV#	CIV#	CIV#	CIV#	CIV#
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

Registers CIV contain the value that was calculated by the CH7016A as the sub-carrier increment value. The entire bit field, CIV[25:0], is comprised of these three registers CIV[23:0] plus CIV[25:24] contained in the CIV Control Register (10h, bits 4 and 5). This value is used when the CIVEN bit is set to '1'. The bit locations are specified below.

Register	Contents
10h	CIV[25:24]
11h	CIV[23:16]
12h	CIV[15:8]
13h	CIV[7:0]

HDTV Mode Register

Symbol: **HDTVM**
Address: **14h**
Bits: **2**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BGBST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HDTV
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	0

HDTV (bit 0) of Register HDTVM toggles between SDTV and HDTV modes.

HDTV = 0 => enables SDTV modes 0 – 47
= 1 => enables HDTV modes 48 – 62

BGBST (bit 7) of Register CB boost the bandgap voltage which controls the DAC output by 6% when set to 1. This has the effect of boosting the DAC output by about 6%. The recommended value is 1.

Clock Mode Register

Symbol: **CM**
Address: **1Ch**
Bits: **4**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	M/S*	MCP	PCM	XCM
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

XCM (bit 0) of Register CM signifies the XCLK frequency for the data input. A value of '0' is used when XCLK is at the pixel frequency (dual edge clocking mode) and a value of '1' is used when XCLK is twice the pixel frequency (single edge clocking mode).

PCM (bit 1) of Register CM controls the P-Out clock frequency. A value of '0' generates a clock output at the pixel frequency, while a value of '1' generates a clock at twice the pixel frequency.

MCP (bit 2) of Register CM controls the phase of the XCLK clock input for the data input. A value of '1' inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching input data.

M/S* (bit 3) of Register CM controls whether the device operates in master or slave clock mode. In master mode (M/S* = '1'), the 14.31818MHz clock is used as a frequency reference in the TV PLL, and the M and N values are used to determine the TV PLL's operating frequency. In slave mode (M/S* = '0') the XCLK input is used as a reference to the TV PLL. The M and N TV PLL divider values are forced to one.

Input Clock Register

Symbol: IC
Address: 1Dh
Bits: 5

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	BLKEN	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	1	0	0	0

XCMD[3:0] (bits 3-0) of Register IC control the delay applied to the XCLK signal before latching input data D[11:0] per the following table. t_{STEP} is given is section 4.5.

Table 31: Delay applied to XCLK before latching input data D[11:0]

XCMD3	XCMD2	XCMD1	XCMD0	Adjust phase of Clock relative to Data
0	0	0	0	0 * t_{STEP}, XCLK ahead of Data
0	0	0	1	1 * t_{STEP}, XCLK ahead of Data
0	0	1	0	2 * t_{STEP}, XCLK ahead of Data
0	0	1	1	3 * t_{STEP}, XCLK ahead of Data
0	1	0	0	4 * t_{STEP}, XCLK ahead of Data
0	1	0	1	5 * t_{STEP}, XCLK ahead of Data
0	1	1	0	6 * t_{STEP}, XCLK ahead of Data
0	1	1	1	7 * t_{STEP}, XCLK ahead of Data
1	0	0	0	0 * t_{STEP}, XCLK behind Data
1	0	0	1	1 * t_{STEP}, XCLK behind Data
1	0	1	0	2 * t_{STEP}, XCLK behind Data
1	0	1	1	3 * t_{STEP}, XCLK behind Data
1	1	0	0	4 * t_{STEP}, XCLK behind Data
1	1	0	1	5 * t_{STEP}, XCLK behind Data
1	1	1	0	6 * t_{STEP}, XCLK behind Data
1	1	1	1	7 * t_{STEP}, XCLK behind Data

BLKEN (bit 6) of Register IC controls the Black Level Register (Register 07h) update during the vertical sync blanking period. A value of '0' disables the Black Level Register update. A value of '1' enables the Black Level Register update.

GPIO Control Register

Symbol: **GPIO**
Address: **1Eh**
Bits: **6**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	GOENB1	GOENB0	GPIOL1	GPIOL0	Reserved	Reserved	POUTE	POUTP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	1	0	0	0	0

POUTP (bit 0) of Register GPIO controls the polarity of the P-Out signal. A value of '0' does not invert the clock at the output pad.

POUTE (bit 1) of Register GPIO enables the P-Out signal. A value of '1' drives the P-Out clock signal out of the P-Out pin. A value of '0' disables the P-Out signal.

GPIOL[1:0] (bits 5-4) of Register GPIO define the GPIO Read or Write Data bits [1:0]. When the corresponding GOENB bits (GOENB[1:0], are '0', the values in GPIOL[1:0] are driven out at the corresponding GPIO pins. When the corresponding GOENB bits are '1', the values in GPIOL[1:0] can be read to determine the level forced into the corresponding GPIO pins. Note that the default state of GPIOLx depends on the state of the GPIOx pins since by default these pins are configured as inputs. With no external pull-up or pull-down the internal pull-up causes GPIOLx to be '1'.

GOENB[1:0] (bits 7-6) of Register GPIO define the GPIO Direction Control bits [1:0]. GOENB[1:0] control the direction of the GPIO[1:0] pins. A value of '1' sets the corresponding GPIO pin to an input, and a value of '0' sets the corresponding pin to a non-inverting output. The level at the output depends on the value of the corresponding bit GPIOL[1:0].

Input Data Format Register

Symbol: **IDF**
Address: **1Fh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	IBS	DES	SYO	VSP	HSP	IDF2	IDF1	IDF0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

IDF[2:0] (bits 2-0) of Register IDF select the input data format for the D[11:0] input. See section 2.3.4 for a listing of available formats.

HSP (bit 3) of Register IDF controls the horizontal sync polarity. A value of '0' defines the horizontal sync to be active low, and a value of '1' defines the horizontal sync to be active high.

VSP (bit 4) of Register IDF controls the vertical sync polarity. A value of '0' defines the vertical sync to be active low, and a value of '1' defines the vertical sync to be active high.

SYO (bit 5) of Register IDF controls the sync direction. A value of '0' defines sync to be input to the CH7016A, and a value of '1' defines sync to be output from the CH7016A.

DES (bit 6) of Register IDF signifies when the CH7016A is to decode embedded sync signals present in the input data stream instead of using the H and V pins. This feature is only available for input data format # 4. A value of '0' selects the H and V pins to be used as the sync inputs, and a value of '1' selects the embedded sync signal.

IBS (bit 7) of Register IDF selects the data and clock input buffer type for the data input D[11:0] according to the following table:

Table 32: D1 Input Buffer Type Selection

IBS	Data Input Buffer Type
0	CMOS, single ended type for clock and data
1	Differential (clock) and comparator (data) type

Connection Detect Register

Symbol: **CD**
Address: **20h**
Bits: **6**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	XOSC2	Reserved	DACT3	DACT2	DACT1	DACT0	SENSE
TYPE:	R/W	R/W	R/W	R	R	R	R	R/W
DEFAULT:	0	1	0	none	none	none	none	0

DACT[3:0] (bits 4-1) and SENSE (bit 0) of Register CD provide a means to sense the connection of a TV to the four DAC outputs. The status bits, DACT[3:0] correspond to the termination of the four DAC outputs. However, the values contained in these status bits ARE NOT VALID until a sensing procedure is performed. Use of this register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits. The detection sequence works as follows:

1) Set the power management register (address 49h) to enable all DACs.
2) Set the SENSE bit to a 1. This forces a constant output from the DACs. Note that during SENSE = 1, these 4 analog outputs are at steady state and no TV synchronization pulses are asserted.
3) Reset the SENSE bit to 0. This triggers a comparison between the voltage present on these analog outputs and the reference value. During this step, each of the four status bits corresponding to individual DAC outputs will be reset to “0” if they are NOT CONNECTED.
4) Read the status bits. The status bits, DACT[3:0] now contain valid information which can be read to determine which outputs are connected to a TV. Again, a “1” indicates a valid connection, a “0” indicates an unconnected output.

XOSC2 (bit 6) of Register CD contains the MSB value for the XOSC (crystal oscillator gain control) word. The entire bit field, XOSC[2:0], is comprised of this bit plus XOSC[1:0] contained in the DAC Control Register (address 21h, bits 7-6).

DAC Control Register

Symbol: DC
Address: 21h
Bits: 7

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	XOSC1	XOSC0	Reserved	SYNCO1	SYNCO0	DACG1	DACG0	DACBP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

DACBP (bit 0) of Register DC selects the DAC bypass mode. A value of '1' outputs the incoming data directly at the DAC[3:0] outputs for the VGA-Bypass RGB output. For the other TV output modes such as S-Video, RCA, SCART and YPrPb, DACBP bit must be set to 0.

DACG[1:0] (bits 2-1) of Register DC control the DAC gain. DACG0 should be set to '0' for NTSC and PAL-M video standards, and '1' for PAL and NTSC-J video standards. DACG1 should be '0' when the input data format is RGB (IDF = 0-3), and '1' when the input data format is YCrCb (IDF = 4). If the output format is HDTV YPrPb, DACG[1:0] should be set as 01, regardless of the input data format.

SYNCO[1:0] (bits 4-3) of Register DC select the signal to be output from the GPIO1/CHSync pin according to **Table 33** below.

Table 33: Composite / Horizontal Sync Output

SYNCO[1:0]	Composite / Horizontal Sync Output
00	No Output
01	VGA Horizontal Sync
10	TV Composite Sync
11	TV Horizontal Sync

XOSC[1:0] (bits 7-6) of Register DC control the crystal oscillator. The entire bit field, XOSC[2:0], is comprised of XOSC[1:0] from this register plus XOSC2 contained in the Connection Detect Register (20h, bit 6).The default value is recommended.

Buffered Clock Output Register

Symbol: BCO
Address: 22h
Bits: 5

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	**SHF2**	**SHF1**	Reserved	BCOEN	BCOP	BCO2	BCO1	BCO0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT: 1Fh	0	0	0	1	0	0	0	1
DEFAULT: 1Dh	0	0	0	0	0	0	0	0

BCO[2:0] (bits 2-0) of Register BCO select the signal output at the BCO pin, according to **Table 34**.

Table 34: BCO Output Signal

BCO[2:0]	Buffered Clock Output	BCO[2:0]	Buffered Clock Output
000	The 14MHz crystal	100	Sine ROM MSB
001	UCLK	101	Cosine ROM MSB
010	VCO divided by K3	110	VGA Vertical Sync
011	Field ID	111	TV Vertical Sync

BCOP (bit 3) of Register BCO selects the polarity of the BCO output. A value of '1' does not invert the signal at the output pad.

BCOEN (bit 4) of Register BCO enables the BCO output pin. When BCOEN is high, the BCO pin will output the selected signal. When BCOEN is low, the BCO pin will be held in tri-state mode.

Reset Register

Symbol: RES
Address: 48h
Bits: 3

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	GPHSS	Reserved	Reserved	ResetIB	ResetDB	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	0	0	0

ResetDB (bit 3) of Register STP resets the datapath. When ResetDB is '0' the datapath is reset. When ResetDB is '1' the datapath is enabled. The datapath is also reset at power on by an internally generated power-on-reset signal.

ResetIB (bit 4) of Register STP resets all control registers (addresses 00h – 7Fh). When ResetIB is '0' the control registers are reset to the default values. When ResetIB is '1' the control registers operate normally. The control registers are also reset at power on by an internally generated power on reset signal.

GPHSS (bit 7) of Register CD controls the selection of the signal on the GPIO1 pin when configured as an output.
GPHSS = 0 => Signal on GPIO1 is GPIOL1 (Register 1Eh, bit 5) when GOENB1 = '0' (Register 1Eh , bit 7)
= 1 => Signal on GPIO1 is HSYNC when GOENB1 = '0' (Register 1Eh , bit 7)

Power Management Register

Symbol: PM
Address: 49h
Bits: 5

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	DACPD3	DACPD2	DACPD1	DACPD0	TVPD
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

TVPD (bit 0) of Register PM controls power down. When TVPD is '0' the CH7016A is ON. When TVPD is '1' the CH7016A is in power down mode.

DACPD[3:0] (bits 4:1) of Register PM control DAC0 through DAC3 Power Down. DAC0 through DAC3 will be turned on only if TVPD bit is set to '0'. If TVPD bit is set to '1', then DAC0 through DAC3 will be in power down state regardless of DACPD0 through DACPD3 state.

Table 35: DAC Power Down Control

TVPD	DACPD[3:0]	Operating State	Functional Description
0	0000	Normal (On)	All DACs on
0	0001		DAC 0 powered down, DACs 1, 2, 3on
0	0010		DAC 1 powered down, DACs 0, 2, 3 on
0	0100		DAC 2 powered down, DACs 0, 1, 3 on
0	1000		DAC 3 powered down, DACs 0, 1, 2 on
1	xxxx	Full Power Down	All circuitry is powered down except serial port

Version ID Register

Symbol: VID
Address: 4Ah
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	1	0	0	0	0	0	0	1

Register VID is a read only register containing the version ID number of the CH7016A family.

Product Number	Version ID
CH7016A	01h

Device ID Register

Symbol: DID
Address: 4Bh
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	1	1	1	0	1

Register DID is a read only register containing the device ID number of the CH7016A family.

Product Number	Device ID
CH7016A	1Ch

WSS Data Register 1

Symbol: **WSSD1**
Address: **4Ch**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	WSSD7	WSSD6	WSSD5	WSSD4	WSSD3	WSSD2	WSSD1	WSSD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Register WSSD1 defines the Wide Screen Signaling data bits [7:0]. The entire bit field, WSSD[19:0], is made up of these bits WSSD[7:0] plus WSSD[15:8] contained in the WSS Data Register 2 (Register 4Dh, bits 7-0) and WSSD[19:16] contained in the WSS Enable Register (Register 4Eh, bits 3-0). See the description for the WSSEN Register (address 4Eh) for more details.

WSS Data Register 2

Symbol: **WSSD2**
Address: **4Dh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	WSSD15	WSSD14	WSSD13	WSSD12	WSSD11	WSSD10	WSSD9	WSSD8
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Register WSSD2 defines the Wide Screen Signaling data bits [15:8]. The entire bit field, WSSD [19:0], is made up of these bits WSSD[15:8] plus WSSD[7:0] contained in the WSS Data Register 1 (Register 4Ch, bits 7-0) and WSSD[19:16] contained in the WSS Enable Register (Register 4Eh, bits 3-0). See the description for the WSSEN Register (address 4Eh) for more details.

WSS Enable Register

Symbol: **WSSEN**
Address: **4Eh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	WSSEN	WSSUVF	WSSS1	WSSS0	WSSD19	WSSD18	WSSD17	WSSD16
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

WSSD[19:16] (bits 3 – 0) of Register WSSEN define the MSBs of the Wide Screen Signaling data bits [19:0]. The entire bit field, WSSD[19:0], is made up of these bits WSSD[19:16] plus WSSD[7:0] contained in the WSS Data Register 1 (Register 4Ch, bits 7-0) and WSSD[15:8] contained in the WSS Data Register 2 (Register 4Dh, bits 7-0). See the description of the WSS modes below for more details.

WSSS[1:0] (bits 5-4) of Register WSSEN select the Wise Screen Signaling mode as shown in **Table 36**.

Table 36: Wide Screen Signaling Formatting

WSSS[1:0]	WSS Mode
00	EIA-J
01	ITU 625 PAL
10	ITU 525 NTSC with CRC code
11	ITU 525 NTSC without CRC code

Mode 0 is designed for 525 line (483i) NTSC systems. The WSS data are inserted on lines 20 and 283. For this mode, the vector WSSD[19:0] (Registers 4Ch – 4Eh) stores WSS data as described by EIAJ CPR-1204. The bits of WSSD[19:14] are the CRC data, which are computed by the user and provided to CH7016A.

Mode 1 is designed for 625 line (576i) PAL systems. The WSS data are on line 23. Only 14 bits of WSSD are used (WSSD[13:0]). For the description of these bits, please refer to ITU-R.BT. 1119 or contact Chrontel.

Both mode 2 and mode 3 are designed for 525 line (483i) NTSC systems. The WSS data are inserted on lines 22 and 285. Only 15 bits of WSSD are used. WSSD[8:0] are information bits while WSSD[14:9] are the CRC bits calculated according to ITU-R.BT.1119. For mode 2, the CRC bits are computed by the user while for mode 3, CH7016A computes the CRC bits. For more details, please contact Chrontel.

WSSUVF (bit 6) of Register WSSEN enables the WSS sine pulse through the back end UV filter.

WSSUVF = 0 => WSS sine pulse bypasses filter
= 1 => WSS sine pulse passes through the UV filter

WSSEN (bit 7) of Register WSSEN enables Wide Screen Signaling.

WSSEN = 0 => WSS disabled
= 1 => WSS enabled

Pedestal Level Control Register

Symbol: PEDL
Address: 4Fh
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	PEDL7	PEDL6	PEDL5	PEDL4	PEDL3	PEDL2	PEDL1	PEDL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	1	1

Register PEDL defines the pedestal. This allows control of the pedestal level independent of the black level. When the input data format is 0 through 3 the correct values are 131 for NTSC and PAL-M, 109 for PAL and 102 for NTSC-J. When the input data format is 4 the correct values are 112 for NTSC and PAL-M, 94 for PAL and 88 for NTSC-J and YPrPb.

I to I Mode Image Enhancement Register

Symbol: **IMIQEN**
Address: **55h**
Bits: **1**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	IQEN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

IQEN (bit 7) of Register ITVLN2 controls the option to sharpen the image quality in modes 37 and 38. When IQEN is set to '1' the image is sharper.

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All power supplies relative to GND	-0.5		5.0	V
	Input voltage of all digital pins	GND – 0.5		VDD + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 seconds)			260	°C
T_{VPS}	Vapor phase soldering (11 seconds)			246	°C
T_{VPS}	Vapor phase soldering (60 seconds)			225	°C

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The temperature requirements of vapor phase soldering apply to all standard and lead free parts.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latch.

4.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	PLL Power Supply Voltage	3.1	3.3	3.6	V
VDD	DAC Power Supply Voltage	3.1	3.3	3.6	V
DVDD	Digital Power Supply Voltage	3.1	3.3	3.6	V
VDDV	I/O Power Supply Voltage	1.1	1.8	3.6	V
R_L	Output load to DAC Outputs		37.5		Ω
T_{AMB}	Ambient operating temperature (Commercial / Automotive Grade 4)	0		70	°C

4.3 Electrical Characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD =3.3V ± 5%)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		33.9		mA
	Video level error			10	%
I_{VDD}	Total supply current		200		mA
I_{VDDV}	VDDV (1.8V) current (15pF load on P-out)		4		mA
I_{PD}	Total Power Down Current		0.06		mA

4.4 Digital Inputs / Outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Inputs		0.25			V
V_{DATAIH}	D[0-11] Input High Voltage		Vref+0.25		DVDD+0.5	V
V_{DATAIL}	D[0-11] Input Low Voltage		GND-0.5		Vref-0.25	V
V_{MISCIH}	GPIOx, RESET* Input High Voltage	DVDD=3.3V	2.7		VDD + 0.5	V
V_{MISCIL}	GPIOx, RESET* Input Low Voltage	DVDD=3.3V	GND-0.5		0.6	V
I_{MISCPU}	Pull Up Current (GPIO, RESET*)	V_{IN} = 0V	0.5		5.0	uA
V_{MISCOH}	GPIOx, BCO, H, V Output High Voltage	I_{OH} = -0.4mA	DVDD-0.2			V
V_{MISCOL}	GPIOx, BCO, H, V Output Low Voltage	I_{OL} = 3.2mA			0.2	V
$V_{P-OUTOH}$	P-OUT Output High Voltage	I_{OH} = - 0.4mA	VDDV-0.2			V
$V_{P-OUTOL}$	P-OUT Output Low Voltage	I_{OL} = 3.2 mA			0.2	V

Note :

V_{DATA} - refers to all digital data (D[11:0]), clock (XCLK, XCLK*) and sync (H, V) inputs. V_{MISC} - refers to GPIOx, and RESET* inputs and GPIOx, BCO/VSYNC outputs and H, V when configured as outputs (SYO=1).

4.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
f_{XCLK}	Input (XCLK) frequency		20		165	MHz
f_{XCLK}	Input (XCLK) frequency		20		27	MHz
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{XJIT}	XCLK clock jitter tolerance			2		ns
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	XCLK = XCLK* to D[11:0], H, V, DE = Vref	0.35			ns
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	D[11:0], H, V, DE = Vref to XCLK = XCLK*	0.5			ns
t_R	Pout, H and V (when configured as outputs) Output Rise Time (20% - 80%)	15pF load DVDD, VDDV = 3.3V			1.50	ns
t_F	Pout, H and V (when configured as outputs) Output Fall Time (20% - 80%)	15pF load DVDD, VDDV = 3.3V			1.50	ns
t_{STEP}	De-skew time increment		50		80	ps

4.6 Timing Information

4.6.1 Clock - Slave, Sync - Slave Mode

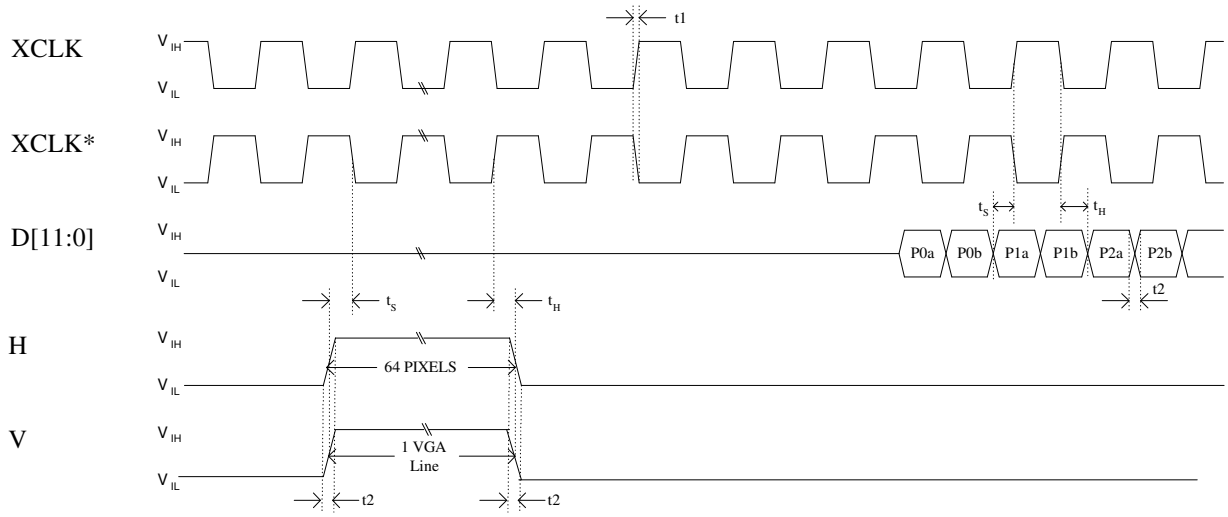

Figure 16: Timing for Clock - Slave, Sync - Slave Mode

Table 37: Timing for Clock - Slave, Sync - Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_H	Hold Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0], H, V rise/fall time w/ 15pF load		1		ns

4.6.2 Clock - Master, Sync - Slave Mode

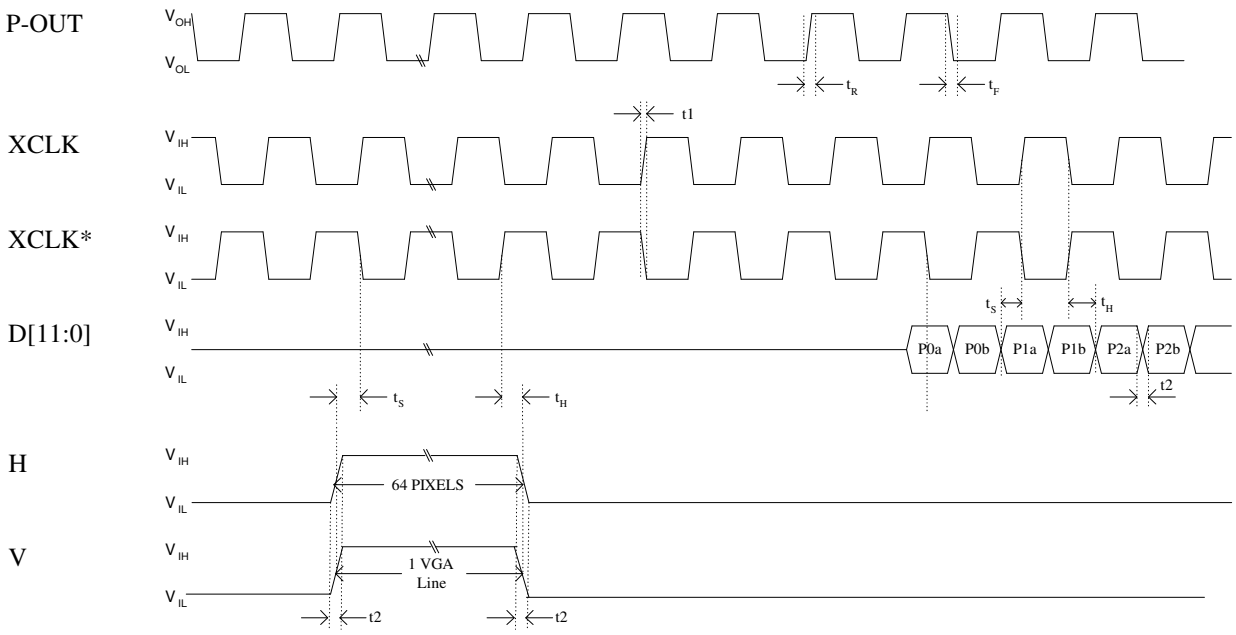

Figure 17: Timing for Clock - Master, Sync - Slave Mode

Table 38: Timing for Clock - Master, Sync - Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_H	Hold Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_R	Pout Output Rise Time	see section 4.5			
t_F	Pout Output Fall Time	see section 4.5			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0], H, V rise/fall time w/15pF load		1		ns

5.5.3 Clock - Master, Sync - Master Mode

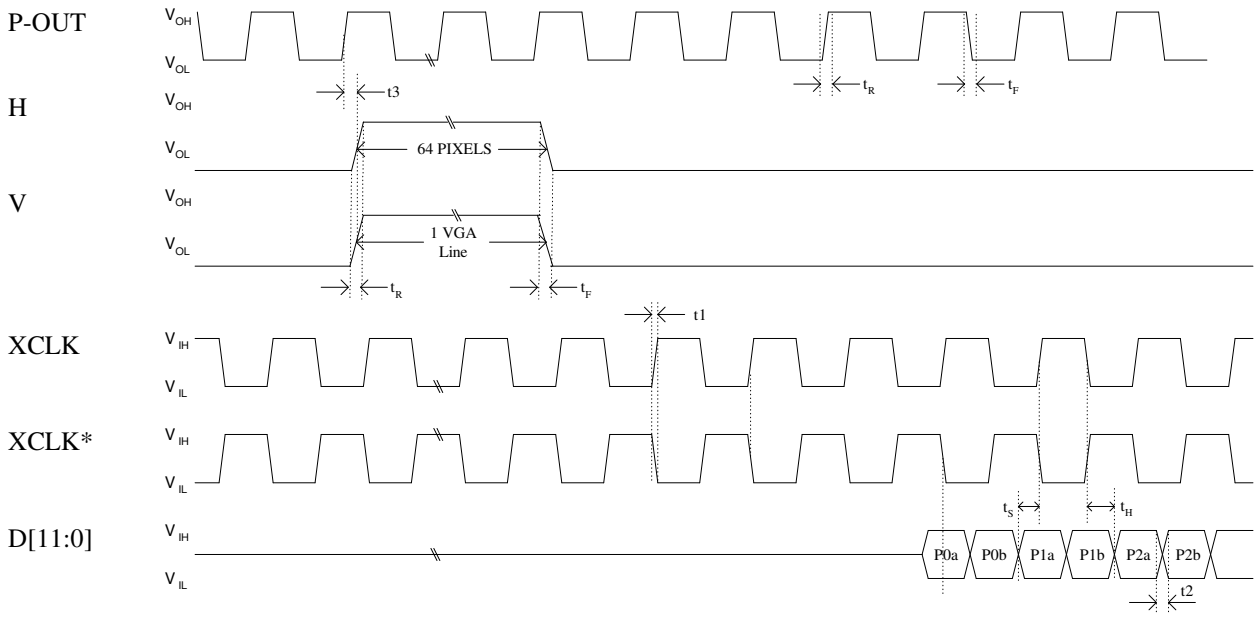

Figure 18: **Clock - Master, Sync - Master Mode**

Table 39: Timing for Clock - Master, Sync - Master Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_H	Hold Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_R	Pout, H, V (when configured as outputs) Output Rise Time	see section 4.5			
t_F	Pout, H, V (when configured as outputs) Output Fall Time	see section 4.5			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0] rise/fall time w/15pF load		1		ns
t3	Hold time: P-OUT to HSYNC, VSYNC delay		1.5		ns

5.0 PACKAGE DIMENSIONS

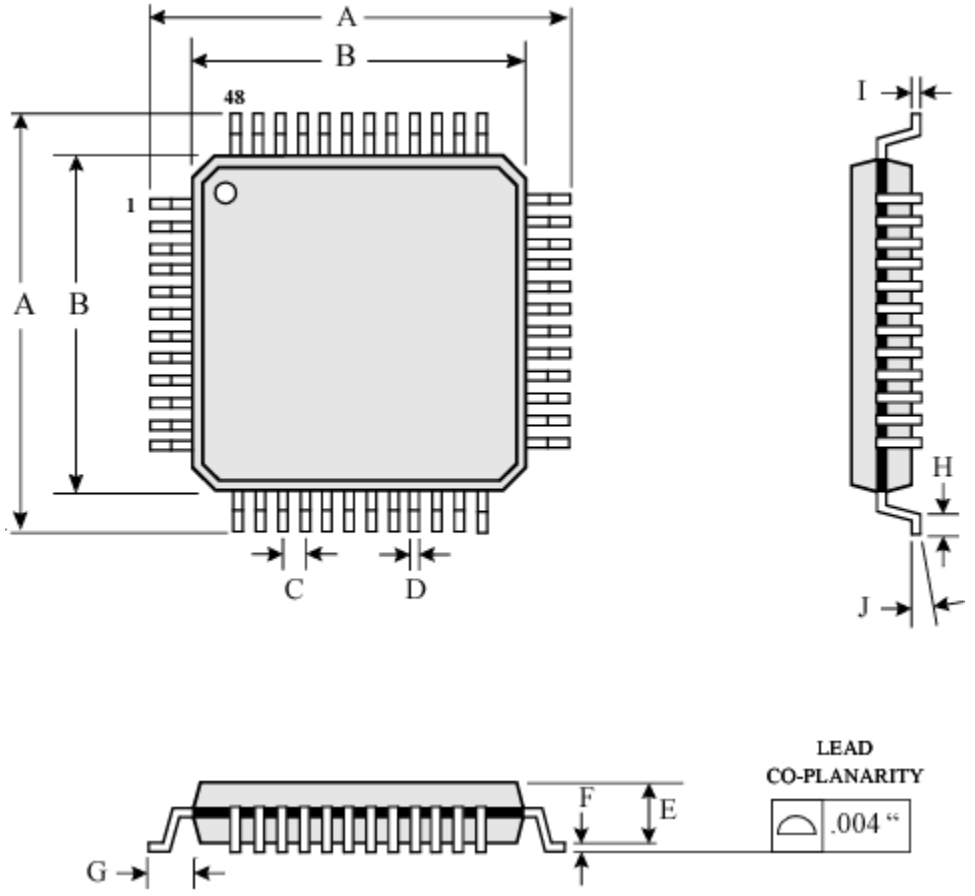

Figure 19: 48 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
48 (7 X 7 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	9	7	0.5	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

6.0 REVISION HISTORY

Table 40: Revisions

Revision #	Date	Section	Description
1.0	3/20/13	All	CH7016A without Macrovision.
1.1	8/29/13	3.3	Change VID and DID number.
1.2	1/7/2014	4.1, 4.2	Move T_{AMB} from 4.1 to 4.2.

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ORDERING INFORMATION

Part Number	Voltage Supply	Pin Type	Package Type	Packaging
CH7016A-DF	3.3V	48	Lead Free LQFP	Tray
CH7016A-DF-TR	3.3V	48	Lead Free LQFP	Tape & Reel

Chrontel

2210 O'Toole Avenue, Suite 100,
San Jose, CA 95131-1326
Tel: (408) 383-9328
Fax: (408) 383-9338
www.chrontel.com
E-mail: sales@chrontel.com