PCB Layout and Design Guide for CH7033B and CH7051B

1.0 INTRODUCTION

Chrontel CH7033B and CH7051B are specifically designed for consumer electronics device and PC markets for which multiple high definition content display formats are required. With its advanced video encoder, flexible scaling engine and easy-to-configure audio interface, the CH7033B and CH7051B satisfies manufactures' products display requirements and reduces their cost of development and time-to-market.

This application note focuses only on the basic PCB layout and design guidelines for CH7033B and CH7051B HDTV/VGA/HDMI/DVI encoder. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 88-pin QFN package of the CH7033B and CH7051B. And in the figures, only HDMI connector will been shown. Please refer to the CH7033B and CH7051B datasheet for the details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7033B and CH7051B should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C2, C4, C5, C7, C8, C10, C11, C13, C14, C16, C18, C19, C22) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7033B and CH7051B ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7033B and CH7051B should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7033B and CH7051B ground pins should be connected to its respective decoupling capacitor ground lead directly, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

The power supply include AVDD, AVDD_DAC, VDDH, AVDD_PLL, VDDIO, DVDD, VDDMQ, VDDMS.
Refer to**Table1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7033B and CH7051B

Pin Assignment	#Of Pins	Type	Symbol	Description
30,41	2	Power	VDDH	DVI/HDMI Power Supply (3.3V)
10,42	2	Power	DVDD	Digital Power Supply (1.8V)
23,46	2	Power	AVDD	Analog Power Supply (3.3V)
73, 77	2	Power	AVDD_DAC	DAC power supply (3.3V)
71	1	Power	AVDD_PLL	PLL Power Supply (1.8V)
53,61	2	Power	VDDMQ	SDRAM output buffer Power Supply (3.3V)
9,60	2	Power	VDDMS	SDRAM Power Supply (3.3V)
33,38	2	Ground	VSSH	DVI/HDMI Ground
83	1	Power	VDDIO	IO Power Supply (1.2-3.3V)
45	1	Ground	DGND	Digital Ground
22,47	2	Ground	AGND	Analog Ground
75, 79	2	Ground	AGND_DAC	DAC Ground
70	1	Ground	AGND_PLL	PLL Ground
52,62	2	Ground	GNDMQ	SDRAM output buffer Ground
59,11	2	Ground	GNDMS	SDRAM Ground

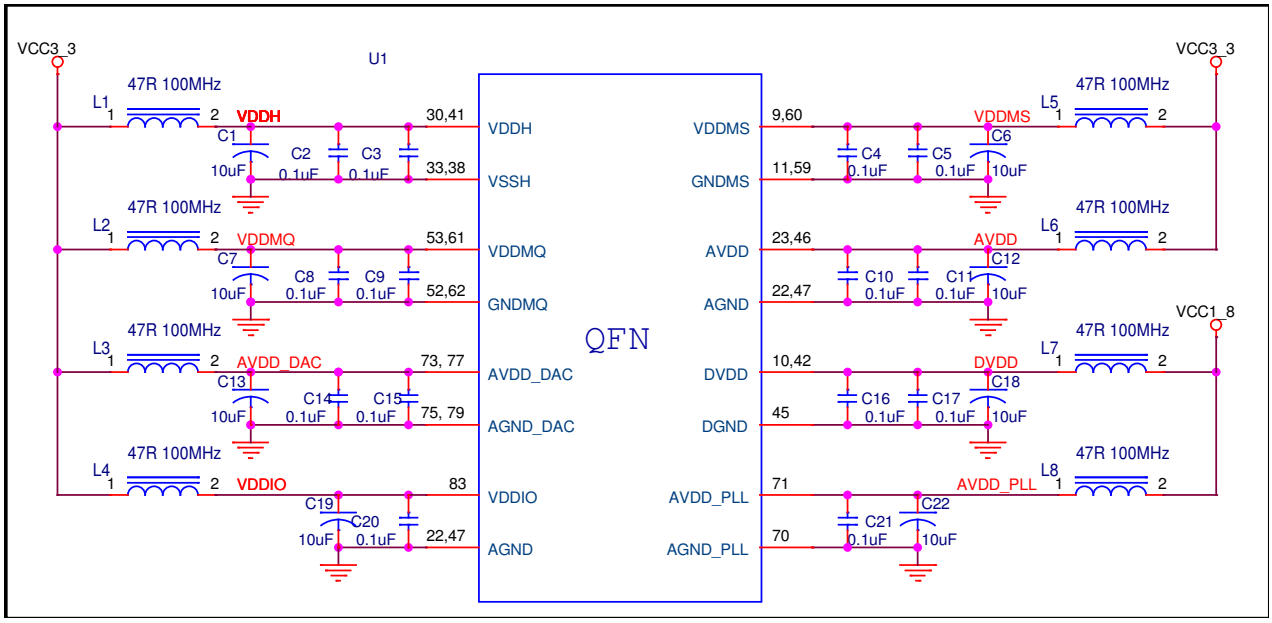


Figure 1: Power Supply Decoupling and Distribution

Note:

1. All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Please refer to Fair Rite part #2743019447 for details or an equivalent part can be used for the diagram.

2.1.3 On chip power-on reset function's sequence

There are two methods for chip power-on reset.
1. The ResetB signal can be generated by on board Resistor and Capacitor delay which can be refer to **Figure 2**. For hard ware circuit, please refer to **2.3 RESETB.**

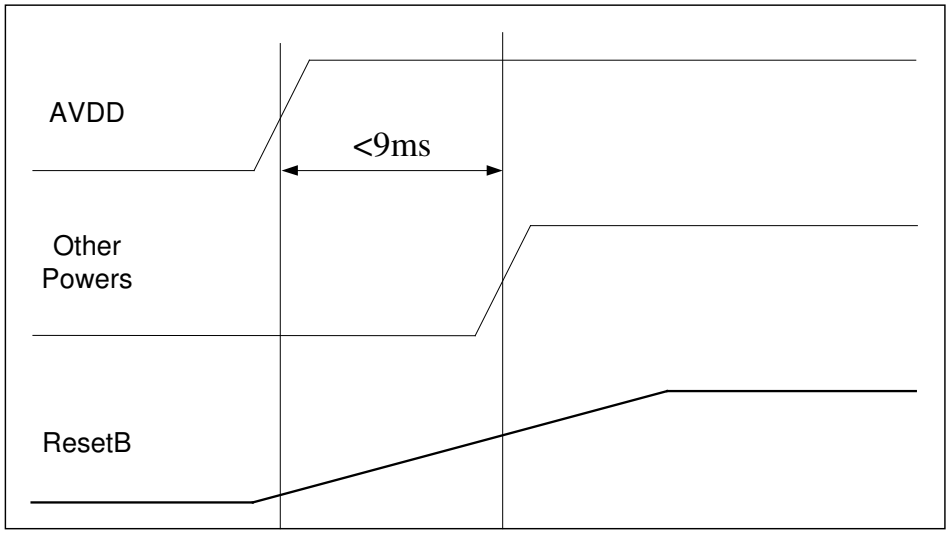


Figure 2: Power-on Reset Function's Sequence on board

2. ResetB signal is generate by system global reset. In this case, the power supply should be valid and stable for at least 20ms before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. Otherwise, the chip can't work well. The timing is shown in **Figure 3.**

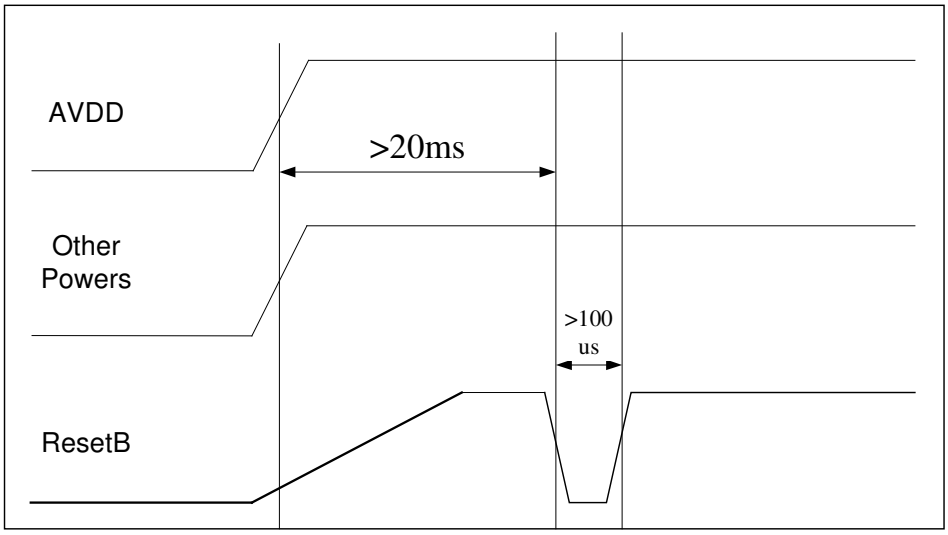


Figure 3: Power-on Reset Function's Sequence external global reset

Note:

1. The rising threshold of RSTB is 2.4V.
2. The falling threshold of RSTB is 0.4V.

2.2 Internal Reference Pins

• ISET pin

This pin sets the DAC current. A 1.2K ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC as shown in **Figure 4**. This resistor should be placed with short and wide traces as near as possible to CH7033B/CH7051B.

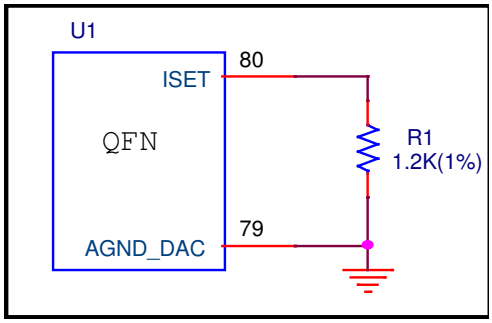


Figure 4: ISET pin connection

2.3 General Control Pins

• RESETB

This pin is the chip reset pin for CH7033B/CH7051B, which is internally pulled-up, places the device in the power on reset condition when this pin is low. A power reset switch can be placed on the RESETB pin on the PCB as a hardware reset for CH7033B/CH7051Bor connect to the system's global reset as shown in **Figure 5**. When the pin is high, the reset function can also be controlled through the serial port.

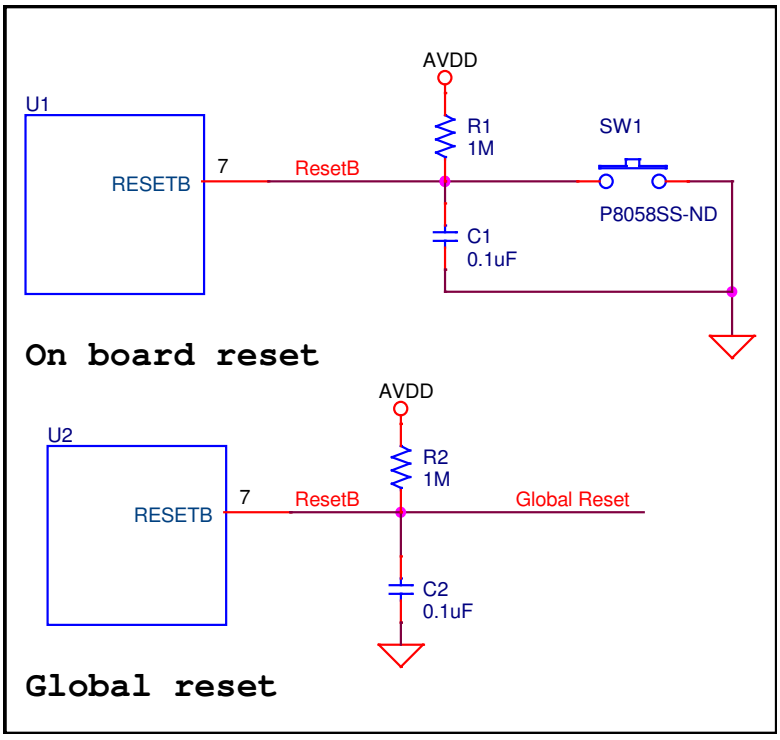


Figure 5: RESETB pin connection

• GPIO

This pin is general purpose input/output. It can be connected to the input signals such as the DE, GCLK, H,V for checking input signals available or achieving other functions.

• XI/FIN and XO

CH7033B and CH7051B have capability to accept external crystal with frequencies from 2.3 MHz to 64 MHz. However, we recommend predefined crystal frequency is 13.5MHz or 27MHz. The crystal must be placed as close as possible to the XI and XO/FIN pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7033B and CH7051B, it is very important that noise should not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7033B and CH7051B.

The crystal load capacitance, C_L, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors **Figure 6** gives a reference design for crystal circuit design.

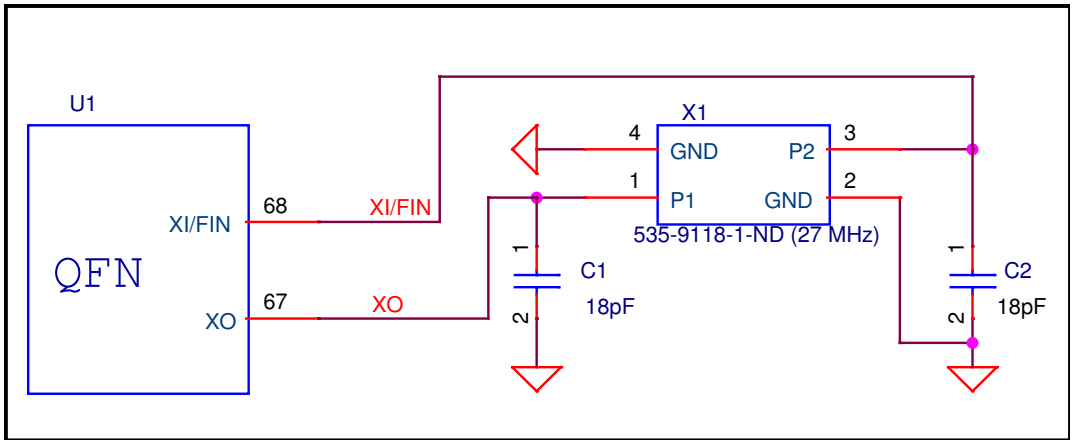


Figure 6: Crystal Pins

• Reference Crystal Oscillator

CH7033B and CH7051B integrate an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7033B and CH7051B. If an external clock source is used, it should be of CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±20 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to CH7033B and CH7051B (C_{ext}).

To be able to tune, a variable capacitor may be connected from XI to ground.

Note that the XI and XO pins each has approximately 10 PF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$$C_{ext} = (2 \times C_L) - C_{int} - 2C_S$$

Where
C_{ext} = external load capacitance required on XI and XO pins.

C_L = crystal load capacitance specified by crystal manufacturer.

C_{int} = capacitance internal to CH7033B and CH7051B (approximately 10-15 pF on each of XI and XO pins).

C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

Such that
$C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int}=2C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int} /2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

2.4 Serial Port Control for CH7033B and CH7051B

• SPC and SPD

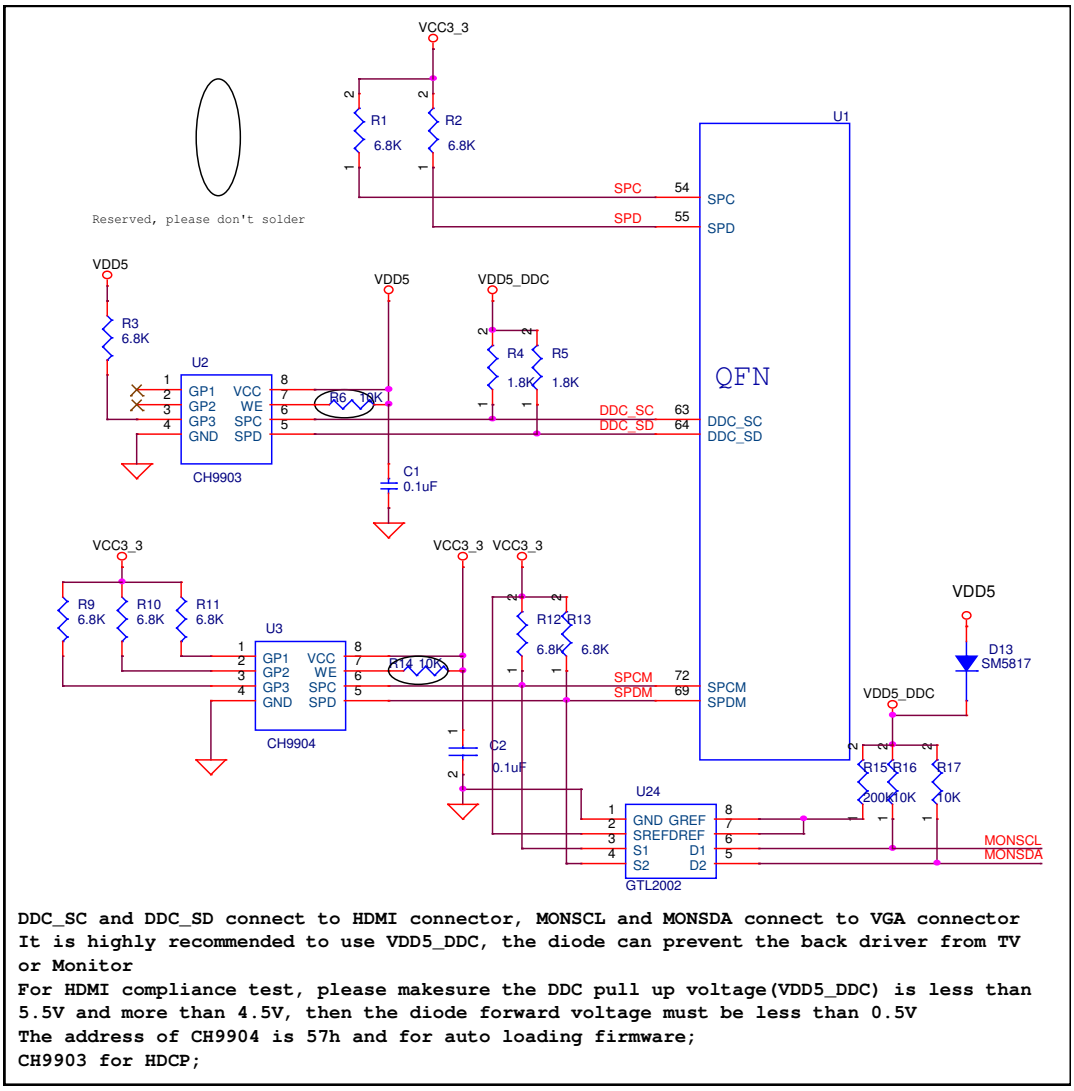
SPD and SPC function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC pins are pulled up to +1.8V ~ +3.3Vwith 6.8 kΩ resistors as shown in **Figure 7**.

• DDC_SC and DDC_SD

DDC_SC and DDC_SD are used to interface with the DDC of DVI/HDMI receiver and the serial PROM. This DDC pair needs to be pulled up to 5V through 1.8 KΩ resistors (Refer to **Figure 7**).

• SPCM and SPDM

SPCM and SPDM can load firmware from external CH9904 BOOT ROM (QFN). In the reference design, SPDM and SPCM pins are pulled up to +3.1V ~ +3.5Vwith 6.8 KΩ resistors as shown in **Figure 7.**
Note: CH9903 hard wire address mustn't be 50h
CH9904 hard wire address should be 57h.



DDC_SC and DDC_SD connect to HDMI connector, MONSCL and MONSDA connect to VGA connector
It is highly recommended to use VDD5_DDC, the diode can prevent the back driver from TV or Monitor
For HDMI compliance test, please makesure the DDC pull up voltage(VDD5_DDC) is less than 5.5V and more than 4.5V, then the diode forward voltage must be less than 0.5V
The address of CH9904 is 57h and for auto loading firmware;
CH9903 for HDCP;

Figure 7: Serial Port Interface: DDC_SC, DDC_SD, SPCM, SPDM and SPC, SPD pins of CH7033B and CH7051B

2.5 Input Pins

• Data Inputs

CH7033B and CH7051B can accept up to 24 data inputs, as shown in **Figure 8**, from a digital video port of a graphics controller. The swing is defined by VDDIO (1.2 ~ 3.3V).
Unused Data input pins should be pulled low with 10kΩ resistors or shorted to Ground directly.

• H/V Sync Pins

The horizontal/vertical sync pins can be used as inputs as shown in **Figure 8**.

• DE/CSB

The DE/CSB pin is used as a data input indicator (Refer to **Figure8**). When the pin is high, the input data is active. When the pin is low, the input data is blanking.
If DE/CSB is not used, it can be left open or pulled down to the Ground.

- **GCLK**

The GCLK input is the clock signal input to the device for using with the H, V, DE and D [23:0] data.

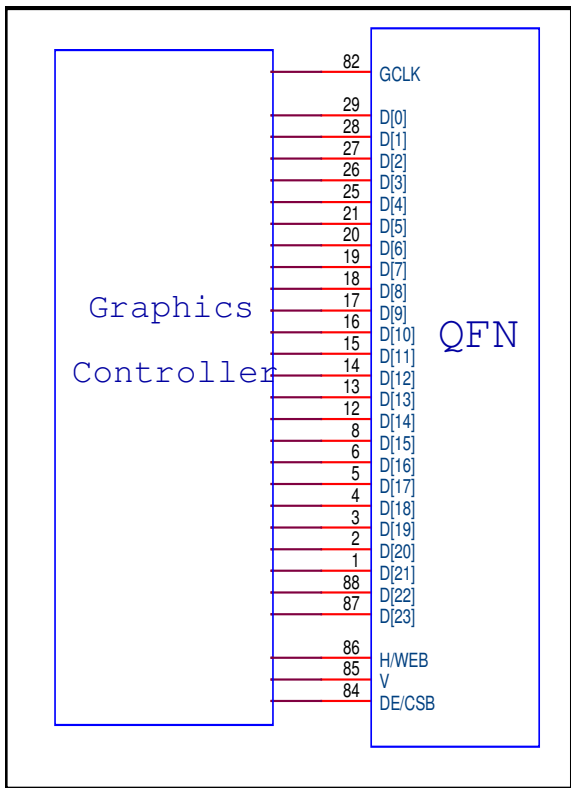


Figure 8: CH7033B and CH7051B Data Input Pins

2.6 SPDIF Interface

SPDIF (pin 56) is an SPDIF audio input pin.

The SPDIF signal to CH7033B and CH7051B is required to be VL<0.4V and VH>2.4V. SPDIF signal has two input ways for CH7033B and CH7051B. SPDIF signal from audio codec is 0-2.5V, then it can be connected to the CH7033B and CH7051B directly; if through a RCA connector, the signal on RCA connector is AC coupled signal, signal level of which is 0.5V to 1V. Therefore, voltage level shifting is strongly recommended. If the current SPDIF circuit is considered too complicated, a simple circuit can be used (Refer to **Figure 9**).

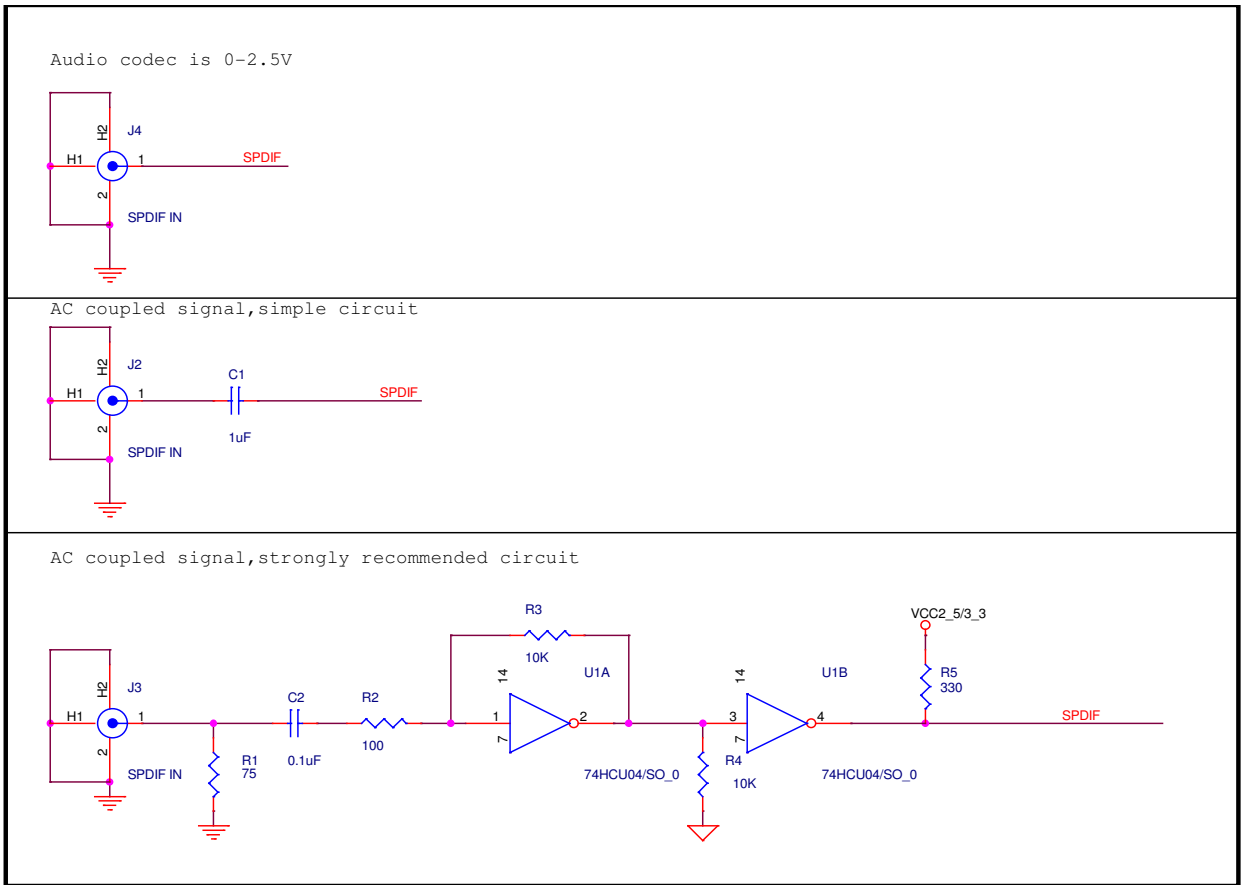


Figure 9: SPDIF pin of CH7033B and CH7051B

2.7 I2S Interface

I2S audio input can be configured through programming CH7033B AND CH7051B registers. An I2S bus design consists of three serial bus lines: a line with data channel [SD], a word select line [WS], and a clock line [SCK]. Data is transmitted two's complement, MSB first.

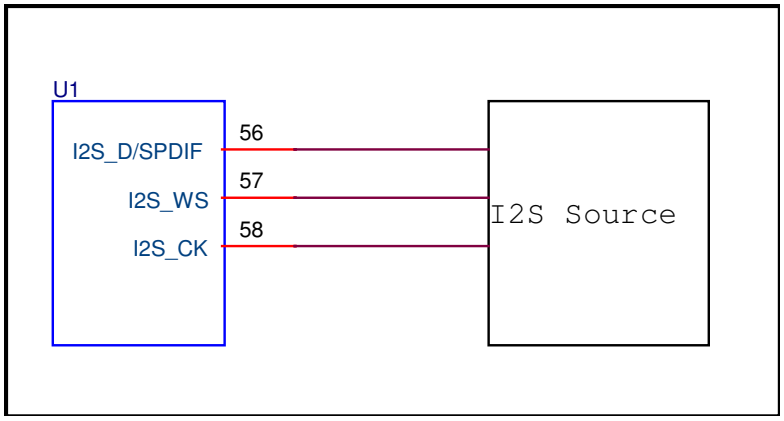


Figure 10: CH7033B and CH7051B I2S Input Pins

2.8 DVI/HDMI Outputs

The TLC, TLC*, TDC [2:0], TDC [2:0]* signals are high frequency differential signals that need to be routed with special precautions. Since those signals are differential, they must be routed in pairs.

2.8.1 Differential Pair Impedance

To match the external cable impedance and maintain the maximal energy efficiency it is important to meet the impedance target of 100 Ω ± 10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thickness, board dielectric, etc. The DVI/HDMI differential pairs should be routed on the top layer directly to the DVI/HDMI connector pads if possible.

2.8.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized; inductive effects may be introduced, causing spikes in the signals. Trace routing lengths from CH7033B and CH7051B to the HDMI/DVI connector are limited to a maximum of 2 inches. The CH7033B and CH7051B should be as close to the HDMI/DVI connector as possible.

2.8.3 Length Matching for Differential Pairs

The HDMI/DVI specifies the intra-pair skew and the inter-pair skew as in **Table 2**. The intra-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between the true and complement signals. The inter-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between any two single-ended data signals that do not constitute a differential pair.

Table 2: Maximum Skews for the HDMI/DVI Transmitter

Skew Type	Maximum at Transmitter
Intra-Pair Skew	0.15 T_{bit}
Inter-Pair Skew	0.20 T_{Pixel}

Where T_{bit} is defined as the reciprocal of Data Transfer Rate and T_{Pixel} is defined as the reciprocal of Clock Rate. Therefore, T_{Pixel} is 10 times T_{bit}. In other words, the intra-pair length matching is much more stringent than the inter-pair length matching.

It is recommended that length matching of both signals of a differential pair be within 5 mils. Length matching should occur on a segment by segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 100 mils.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

2.8.4 ESD Protection for HDMI/DVI Interface

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each DVI/HDMI Output (data and clock).

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel's recommended diode protection circuitry, using SEMTECH Rclamp0524P diode array devices, will protect the CH7033B and CH7051B device from DVI/HDMI panel discharges of greater than 8kV (contact) and 16kV (air). The RClamp0524P have a typical capacitance of only 0.30pF between I/O pins. This low capacitance won't bring too much bad effect on DVI/HDMI eye diagram test.

Figure11(A) and **(B)** show the connection of DVI/HDMI connectors, including the recommended design of SEMTECH Rclamp0524P diode array devices. DVI/HDMI connector is used to connect the CH7033B and CH7051B DVI/HDMI outputs to the display panels.

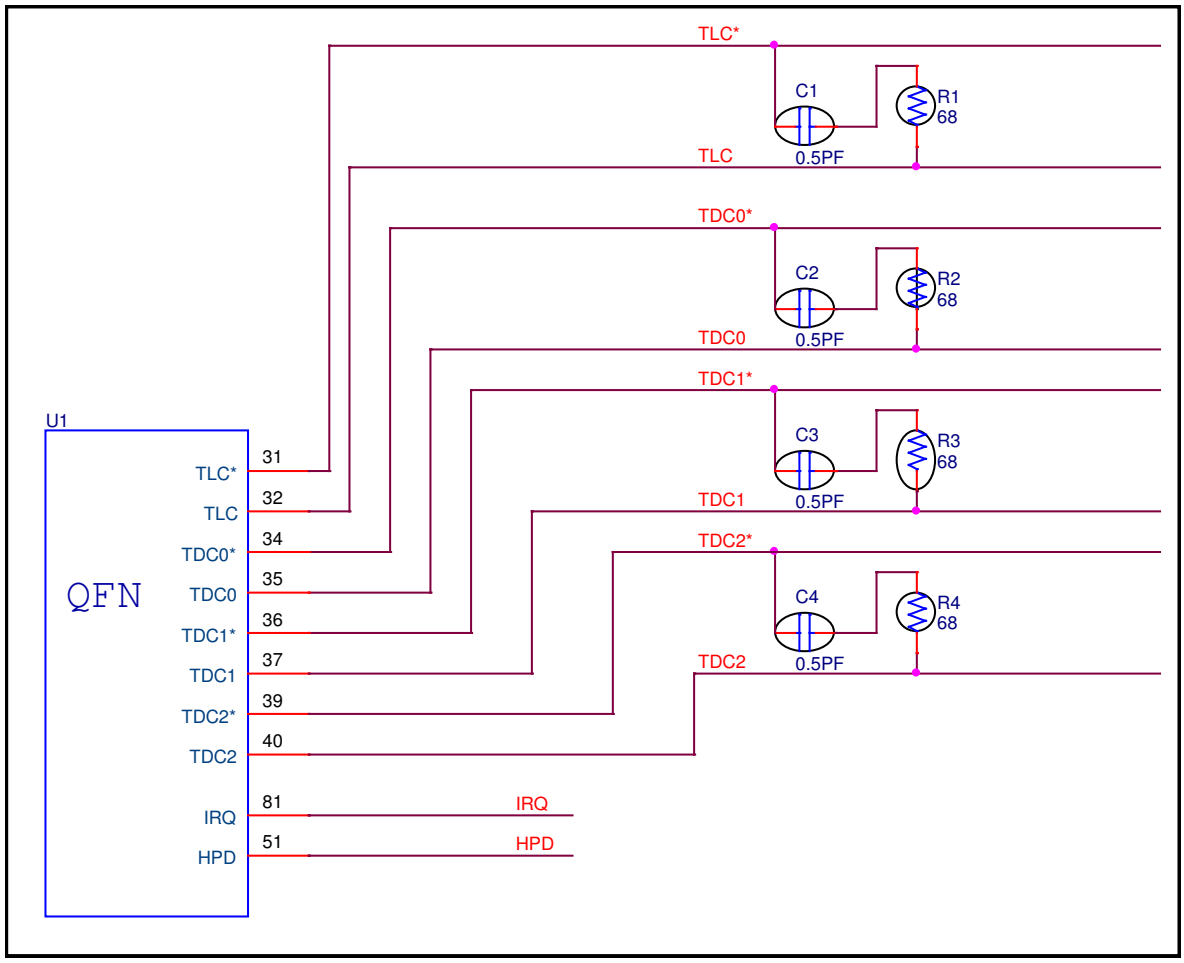


Figure 11(A): The connection of the DVI/HDMI outputs

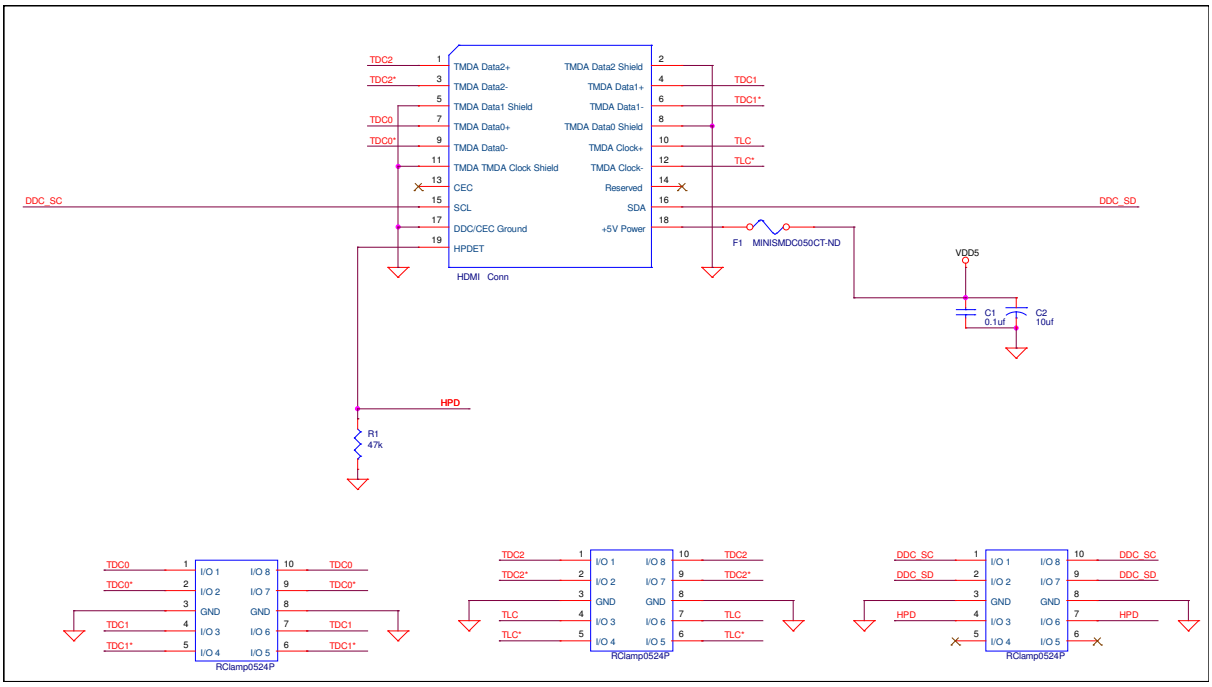


Figure 11(B): The connection of the HDMI outputs－CH7033B and CH7051B HDMI connectors

The following is the description for each DVI/HDMI interface pins

• DVI/HDMI Link Data Channel (TDC [2:0] and TDC [2:0]*)

These pins provide DVI/HDMI differential outputs for data channel 0 (blue), data channel 1 (green) and data channel 2 (red). It is recommended that an impedance compensation circuit be added for each differential pair, including DVI/HDMI Clock outputs (Refer to **Figure 11 (A)**).

• DVI/HDMI Link Clock Outputs (TLC and TLC*)

These pins provide the DVI/HDMI differential clock outputs for DVI/HDMI corresponding to data on the TDC [2:0] and TDC [2:0]* outputs (Refer to **Figure 11 (A)**).

• HPD (DVI/HDMI Hot Plug Detect)

This input pin determines whether the DVI/HDMI link is connected to a DVI/HDMI panel. When the panel is connected, the HPD will be given a voltage greater than 2.4 volts. Refer to **Figure 11 (B)** for the design example.

• IRQ

This pin should be connected with graphic controller directly.

2.9 Video Output

- **YPbPr and RGB + Csync output**

CH7033B and CH7051B support both RGB+Csync and HDTV YPbPr output format. The resolution is from 480P to 720P 1080i and 1080P. In RGB+Csync output format, the Csync high level is the same with AVDD power supply. Csync pin is a COMS push-pull output pin, customer can use other circuit to change is high level to 0.7V or other voltage level according to different Receivers. (Refer to **Figure 12**)

- **VGA output**

VGA standard output signal level of Hsync and Vsync is more than 2.4V. CH7033B and CH7051B Hsync and Vsync output signal level is same with AVDD power supply. Customer can use 74ACT08 (AND GATE) to pull high this signal level to 5V(recommend to add the diode). It is recommended but not necessary. (Refer to **Figure 12**)

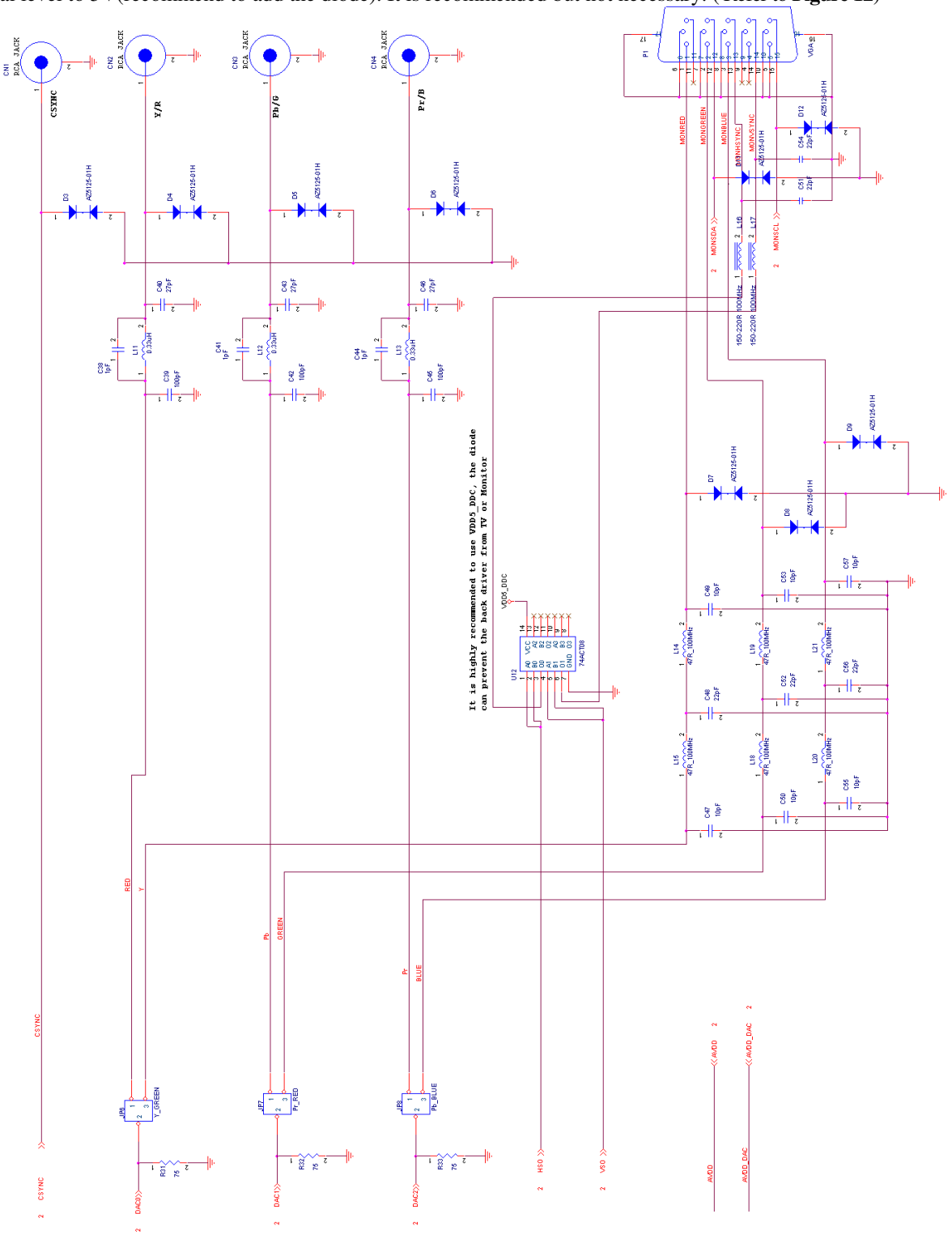


Figure 12: CH7033B AND CH7051B YpbPr, RGB+Csync and VGA output

Note: In order to minimize the hazard of ESD, a set of protection diodes (AZ5125-01H) are highly recommended for each DAC and Sync Output.

2.10 Thermal Exposed Pad Package

The CH7033B and CH7051B are available in 88-pin QFN package with thermal exposed pad package. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7033B and CH7051B.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 14**.

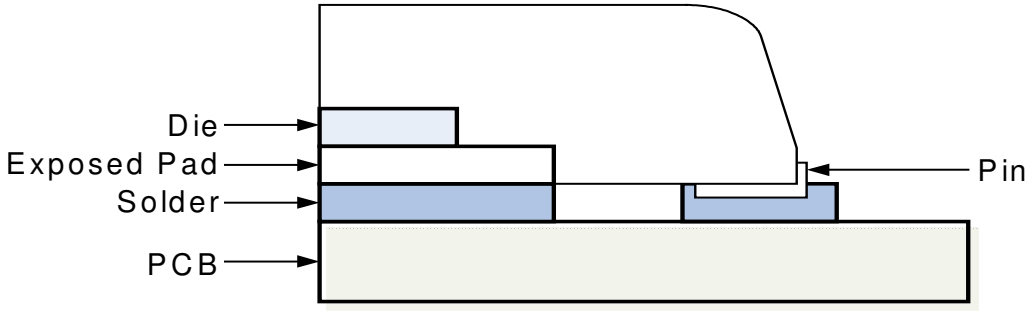


Figure 14: Cross-section of exposed pad package

Thermal pad dimension is from 6.6mm to 6.9mm (min to max), 6.6mm x 6.6mm is the minimum size recommended for the thermal pad, and 6.9mm x 6.9mm is the maximum size. The thermal land pattern should have a 5x5 grid array of 1.0 mm pitch thermal vias connected to the ground layer of the PCB. These vias should be 0.3mm in diameter with 1 oz copper via barrel plating. Please refer to **Figure 15**.

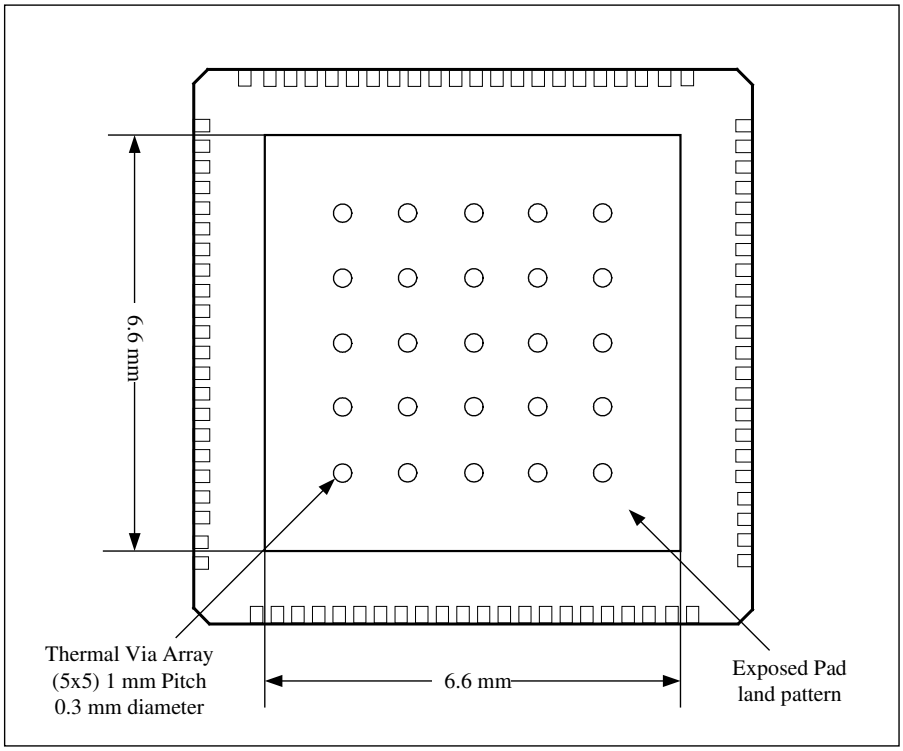


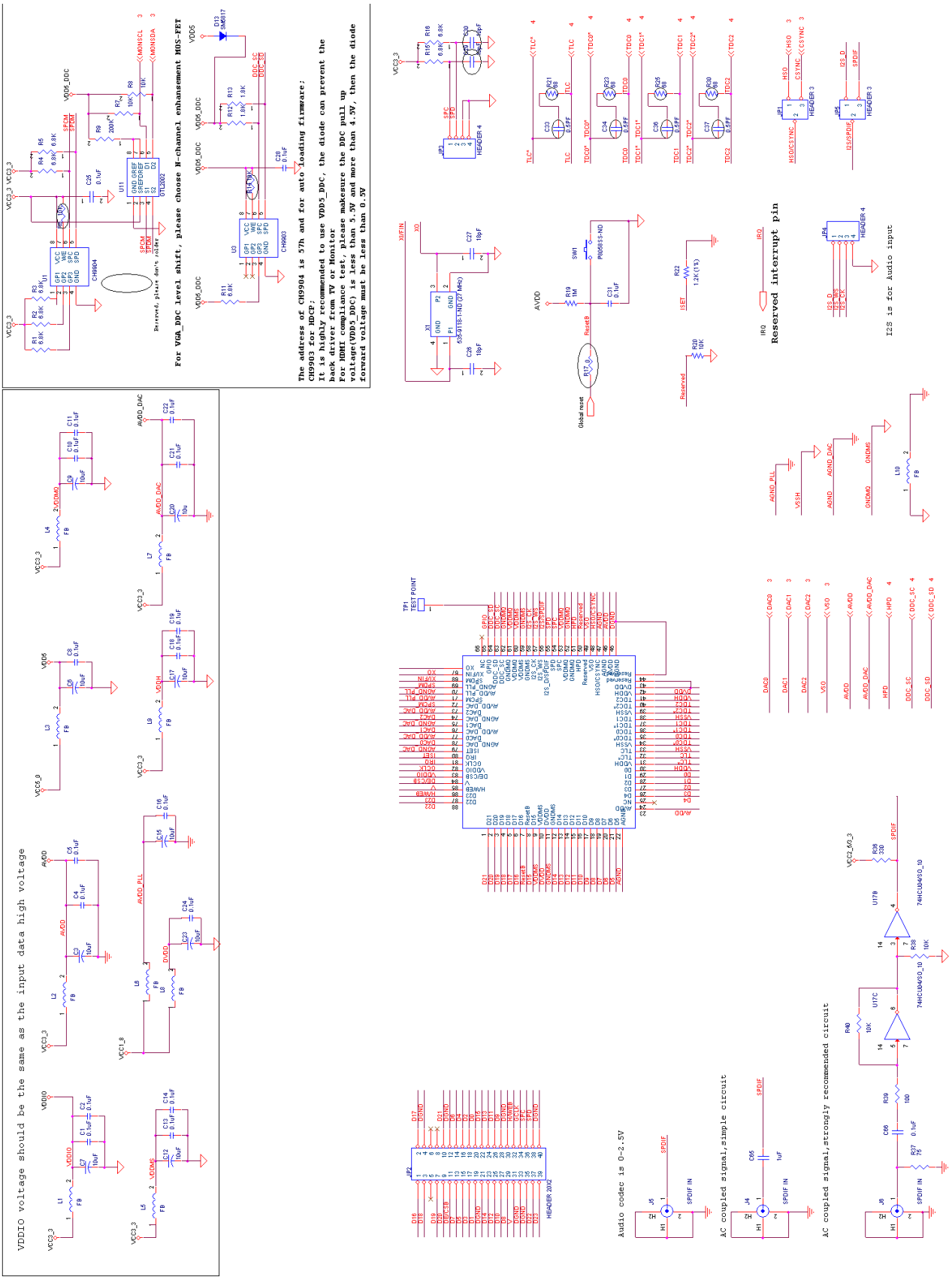
Figure 15: Thermal Land Pattern

When applying solder paste to the thermal land pattern, the recommended stencil thickness is from 5 to 8 mils. Thermal resistance was calculated using the thermal simulation program called ANSYS.

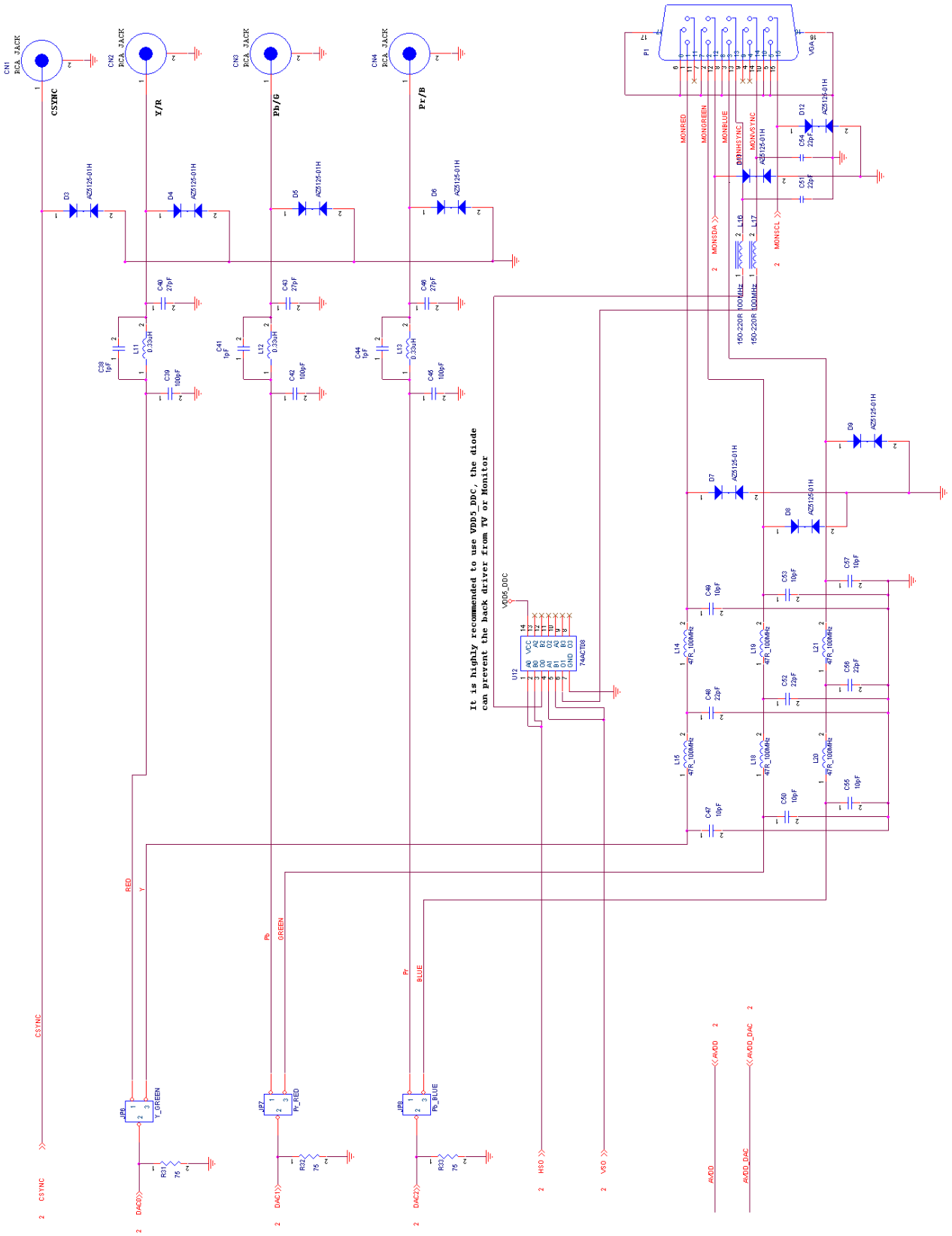
3.0 REFERENCE DESIGN EXAMPLE

The figures below are the reference schematic of CH7033B and CH7051B, which is provided here for design reference only. Please contact Chrontel Applications group if necessary. **Table 3** provides the BOM list for the reference schematic.

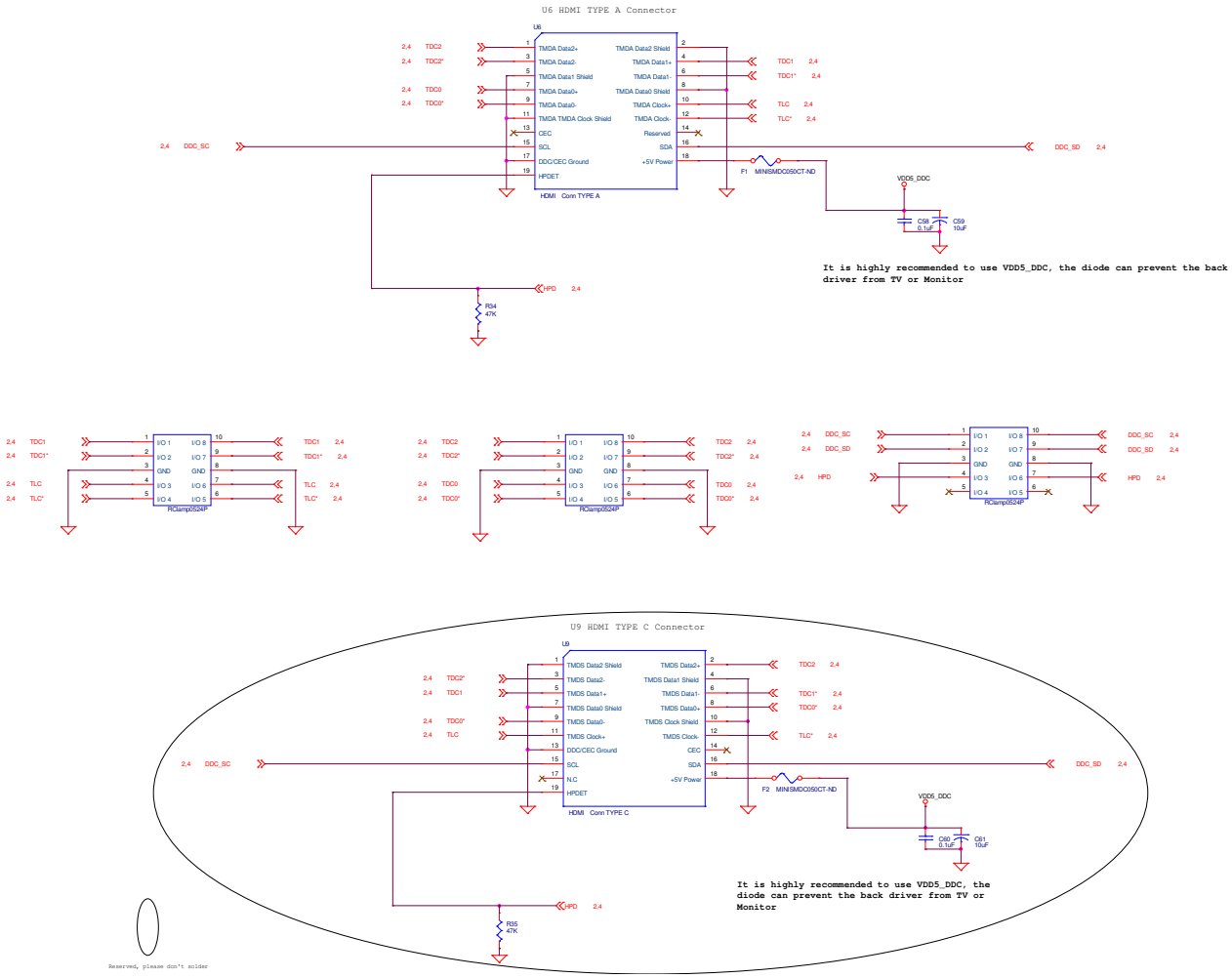
3.1 Reference Schematic



(a) QFN connection



(b) YpbPr, RGB+Csync and VGA output



(c) HDMI output

3.2 Reference Board Preliminary BOM

Table 3: CH7033B AND CH7051B Reference Design BOM List

Item	Quantity	Reference	Part
1	9	D3, D4, D5, D6, D7, D8, D9,D11, D12	AZ5125-01H
2	1	D13	SM5817
3	20	C1, C2, C4, C5, C8, C10, C11, C13, C14, C16, C18, C19, C21, C22, C24, C25, C28, C35, C58, C60	0.1uF
4	11	C3, C6, C7, C9, C12, C15, C17, C20, C23, C59, C61	10uF
5	3	C38, C41, C44	1PF
6	8	C29, C30, C47, C49, C50, C53, C55, C57	10pF
7	2	C26, C27	18pF
8	5	C48, C51, C52, C54, C56	22pF
9	3	C39, C42, C45	100pF
10	3	C40, C43, C46	27pF
11	2	C31, C32	1uF
12	4	C33, C34, C36, C37	0.5PF
13	2	F1, F2	MINISMDC050CT-ND
14	2	JP3, JP4	Header 4
15	1	JP2	Header 20x2
16	5	JP1. JP5, JP6, JP7, JP8	Header 3
17	7	J1, J2, J3, CN1, CN2, CN3, CN4	RCA
18	12	L1, L2, L3, L4, L5, L6, L7, L8, L9, L10, L16, L17	FB
19	3	L11, L12, L13	0.33uH
20	6	L14, L15, L18, L19, L20, L21	47 Ω_100M
21	1	P1	VGA
	8	R1, R2, R3, R4, R5, R11, R15, R16	6.8 k Ω
23	1	R17	0 Ω
24	1	R19	1MΩ
25	1	R9	200K
26	1	R22	1.2 k Ω (1%)
27	7	R6, R7, R8, R14, R20, R24, R29	10 k Ω
28	2	R12, R13	1.8 k Ω
29	1	R27	330 Ω
30	1	R28	100 Ω
31	4	R26,R31,R32,R33	75 Ω
32	2	R34, R35	47k Ω
33	4	R21, R23, R25, R30,	68 Ω
34	1	SW1	P8058SS-ND
35	1	U1	CH9904
36	1	U2	CH7033B or CH7051BA
37	1	U3	CH9903
38	1	U4	74HCU04/SO_10
39	1	U12	74ACT08
40	1	U6	HDMI connector TYPEA
41	3	U7, U8, U16	Rclamp0524P
42	1	U9	HDMI connector TYPEC
43	1	X1	535-9118-1-ND (27MHz)
44	1	U11	GTL2002

4.0 REVISION HISTORY

Table 4: Revisions

Rev. #	Date	Section	Description
1.0	05/24/2010	All	Initial release
1.1	10/14/2010	DVI/HDMI layout	Add DVI/HDMI layout guide
1.2	03/21/2011	CH7033B AND CH7051B	Modify reference schematic
1.3	07/11/2011	2.1 2.3 2.4 2.10 3.1 3.2	Add 2.1.2 Note and power on sequence Modify figures and add GPIO pin Modify figure Add thermal Exposed Pad Package Modify reference schematic Modify BOM list
1.4	08/08/2011	2.1.3 2.3 2.4 2.8.4 2.9 3.1 3.2	Update power-on reset function's sequence Update RESETB schematic Update schematic of DDC and SPCM, SPDM Update the connections of HDMI output Add description of HDMI Multiplex with VGA Update reference schematic Update BOM list
1.5	08/30/2011	2.1.3 2.3 2.9 3.1 3.2	Update power-on reset function's sequence Update RESETB schematic Update VGA output Update reference schematic Update BOM list
1.6	09/08/2011	2.1.3 2.3 3.1 3.2	Update power-on reset function's sequence Update RESETB schematic Update reference schematic Update BOM list
1.7	06/15/2012	3.1 3.2	Update reference schematic Update BOM list

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