
CH7036 LVDS to HDMI/VGA/LVDS Converter

FEATURES

- Single channel 18-bit/24-bit LVDS receiver and transmitter support display resolution up to 1366x768
- HDMI Transmitter are compliant with HDMI 1.4 specification and DVI 1.0 specification
- HDMI Tx supports up to 1920x1080@60Hz
- Supports VGA display up to 1080p
- DDC master for reading EDID
- Supports Hot Plug Detection (HPD) for HDMI/DVI
- Optional HDCP specification version 1.4 function
- Three 10-bit high speed DACs
- DACs can be switched off through programming internal registers. A separated composite sync is supported
- Monitor connection detection capability. Connection status can be retrieved through device's internal registers
- Pixel-level color enhancement for brightness and contrast (analog RGB only)
- SPDIF audio interface supports up to 20-bit data stream 192kHz/2ch
- Supports I2S digital audio input up to 24-bit data stream (32kHz/2ch, 44.1kHz/2ch, 48kHz/2ch, 88.2kHz/2ch, 96kHz/2ch, 176.4kHz/2ch and 192kHz/2ch)
- On-chip frame buffer allows flexible input LVDS video timing.
- Capable of converting input video frame rate to satisfy external displays' refresh rate requirements
- Advanced scaling engine to upsize/downsize display resolution for HDMI, DVI and analog RGB outputs
- Programmable adaptive de-flickering filter
- Image display rotation supports for HDMI/DVI and analog RGB outputs. The screen display can be rotated 90/180/270 degree or flipped either horizontally or vertically
- Horizontal/vertical position shifting for the VGA display is programmable
- Flexible crystal or oscillator clock input frequency for analog RGB output (2.3MHz – 64MHz). 27 MHz external crystal is recommended for HDMI output.
- IO and SPC/SPD supply voltages from 1.8V to 3.3V
- Programmable power management

GENERAL DESCRIPTION

The CH7036 is specifically designed for Consumer Electronics Devices and Personal Computers that require High Definition (HD) Content video playback on the external displays such as HDMI/DVI monitors.

The CH7036's HDMI transmitter is designed to support 1080p HDTV. For desktop monitors that do not have the HDMI input, the CH7036 has the capability to disable HDMI mode and output DVI signal or analog RGB signal (VGA). To support multi-display, the CH7036 can output either HDM/DVI or Analog RGB signals together with LVDS signal pass-through.

The CH7036's single channel LVDS receiver/transmitter complies with the SPWG specification, a popular LVDS standard used by panel manufacturers. Each input/output LVDS interface is equipped with 4/1 pairs of differential signal buses to support video data and clock. The built-in dithering mechanism can be applied to approximate true 24-bit color video data if system manufacturers use less expensive 18-bit panels. Conversely, if input data is only 18-bit color, the simulation to 24-bit color for high-end TFT LCD is also supported.

The device's LVDS receiver can accept maximum video clock frequency for up to 85MHz or 1366x768 resolution in 24-bit color per pixel. A powerful scaling engine working together with other video processing circuits, will convert the captured LVDS signal stored in the internal SDRAM into High Definition Content video data. The built-in mixer will combine this HD digital RGB signal with decoded audio stream into HDMI format data, which will be serialized for output display by the CH7036 TMDS encoder.

The CH7036 supports both SPDIF and 2-channel I2S digital audio inputs. Its high fidelity audio decoder engine has the capability of sampling audio frequencies for up to 192kHz for 2 channels.

Utilizing its high speed internal frame buffer, the CH7036's scaling engine can increase the flexibility of the screen display. The video enhancement includes resizing the HDMI/DVI and RGB output display resolution, performing Frame Rate Conversion as well as rotating display orientation. Other video fine tuning, such as brightness control or contrast adjustment can be used to improve the display on the analog RGB monitor.

When CH7036 is powered up, its MCU is able to automatically execute the device configuration software

- The device is fully programmable through serial port or can automatically load firmware from ChronTEL Boot ROM (CH9904)
 - Offered in 88-pin QFN package
- in the device’s internal memory. When the firmware in the memory is programmed to support EDID communication and HPD, the MCU will toggle DDC bus lines to retrieve the display timing from the HDMI/DVI monitor if HPD is asserted. Furthermore an interrupt signal can be generated by MCU to host while the CH7036’s HPD is high.

APPLICATIONS

- Netbooks
- MIDs
- Tablet PCs
- Industrial PCs

The CH7036 supports the optional HDCP feature for preventing illegally copy High Definition Contented media.

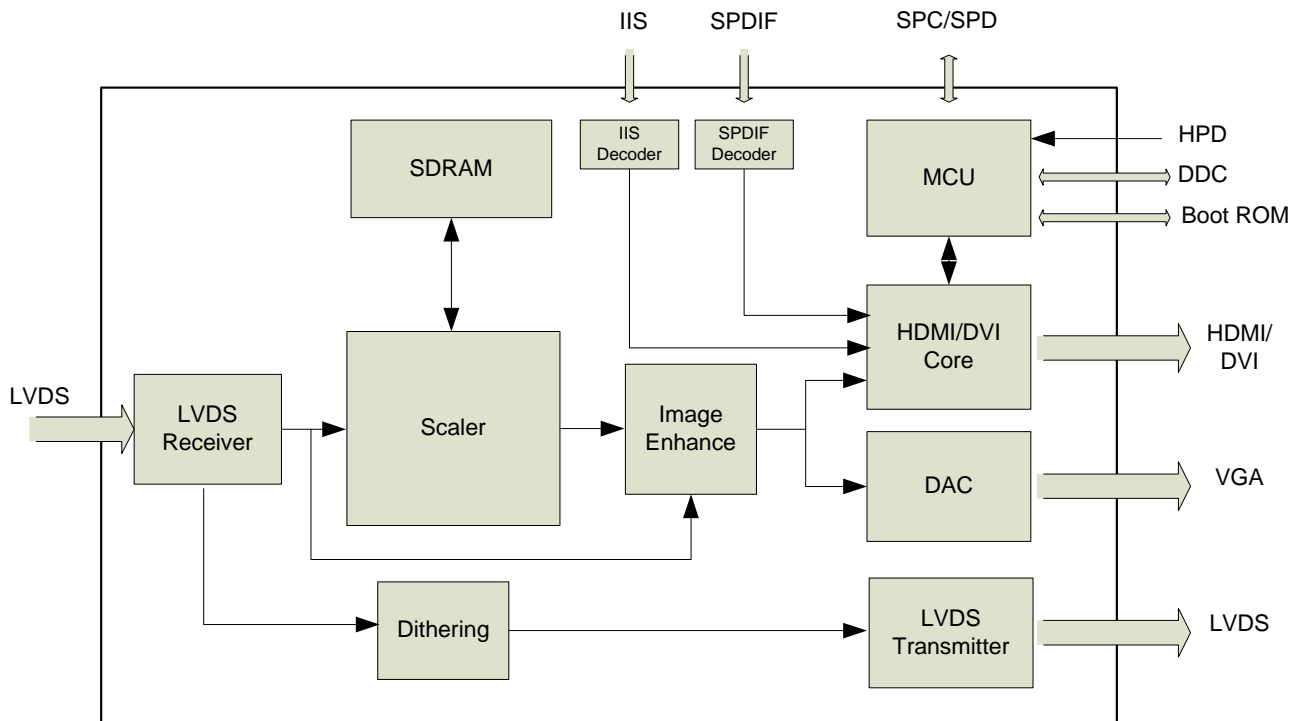


Figure 1: Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

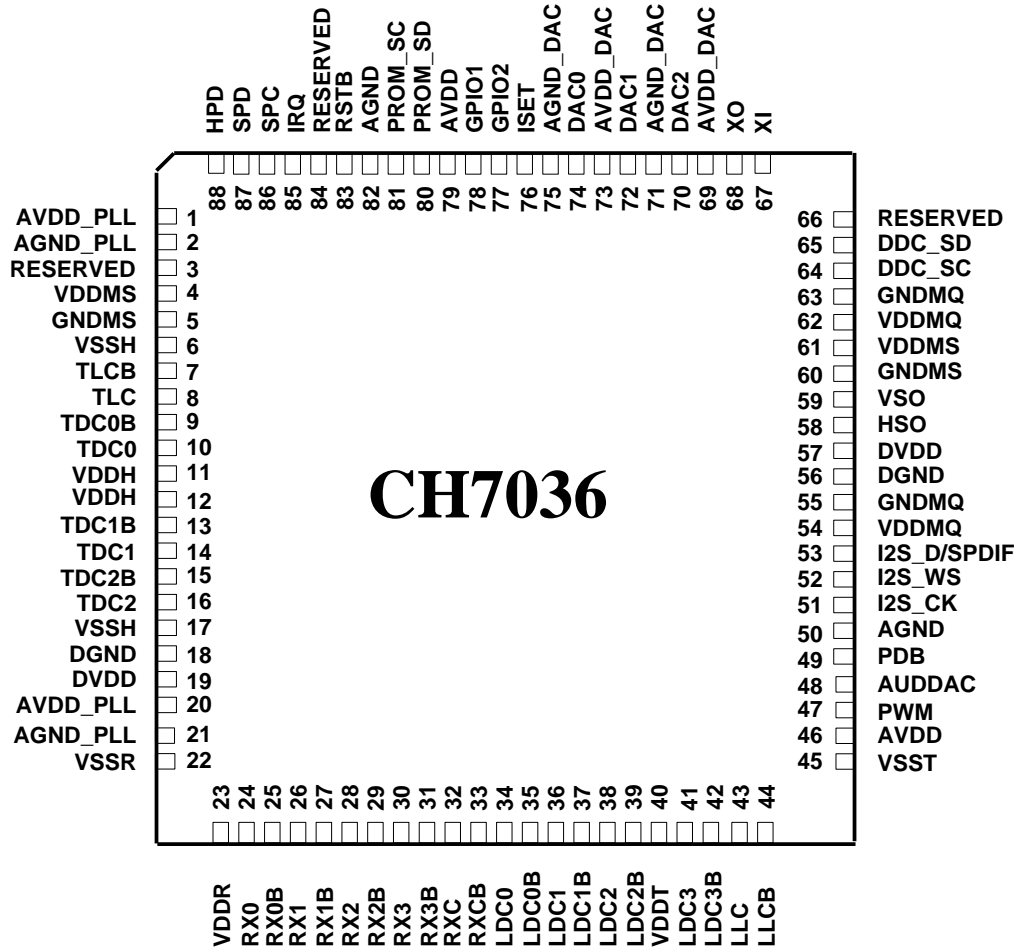


Figure 2: Pin Out

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
3	In	RESERVED	Reserved Pin. This pin should be pulled low with a 10 kΩ resistor
7,8	Out	TLCB/TLC	HDMI Clock Outputs These pins provide the differential clock output for the HDMI
9,10	Out	TDC0B/TDC0	HDMI Data Channel 0 Outputs These pins provide the HDMI differential outputs for data channel 0
13,14	Out	TDC1B/TDC1	HDMI Data Channel 1 Outputs These pins provide the HDMI differential outputs for data channel 1
15,16	Out	TDC2B/TDC2	HDMI Data Channel 2 Outputs These pins provide the HDMI differential outputs for data channel 2
24,25	In	RX0/RX0B	LVDS Data Channel 0 Inputs

			These pins provide the LVDS differential inputs for data channel 0
26,27	In	RX1/RX1B	LVDS Data Channel 1 Inputs These pins provide the LVDS differential inputs for data channel 1
28,29	In	RX2/RX2B	LVDS Data Channel 2 Inputs These pins provide the LVDS differential inputs for data channel 2
30,31	In	RX3/RX3B	LVDS Data Channel 3 Inputs These pins provide the LVDS differential inputs for data channel 3
32,33	In	RXC/RXCB	LVDS Clock Inputs These pins provide the LVDS differential input clocks
34,35	Out	LDC0/LDC0B	LVDS Data Channel 0 Outputs These pins provide the LVDS differential outputs for data channel 0
36,37	Out	LDC1/LDC1B	LVDS Data Channel 1 Outputs These pins provide the LVDS differential outputs for data channel 1
38,39	Out	LDC2/LDC2B	LVDS Data Channel 2 Outputs These pins provide the LVDS differential outputs for data channel 2
41,42	Out	LDC3/LDC3B	LVDS Data Channel 3 Outputs These pins provide the LVDS differential outputs for data channel 3
43,44	Out	LLC/LLCB	LVDS Clock Outputs These pins provide the LVDS differential output clocks
47	Out	PWM ^[1]	Backlight Brightness Adjustment
48	Out	AUDDAC ^[1]	Audio Control Output Pin
49	Input	PDB	Power Down the Whole Chip High: Power on CH7036; Low: Power down CH7036
51	In	I2S_CK	I2S Clock Signal
52	In	I2S_WS	I2S Channel Select Signal
53	In	I2S_D/SPDIF	SPDIF Audio Signal Input. In default, this pin is configured to SPDIF audio signal input I2S Data Input. I2S audio input can be configured through programming CH7036 registers
58	Out	HSO	Analog RGB Horizontal Sync Output
59	Out	VSO	Analog RGB Vertical Sync Output
64	Out	DDC_SC ^[2]	Serial Port Clock Output to DDC This pin functions as the clock bus of the serial port to HDMI or DVI DDC receiver. This pin will require a pull-up 1.8 kΩ resistor to +5V
65	In/Out	DDC_SD ^[2]	Serial Port Data to DDC This pin functions as the bi-directional data pin of the serial port to HDMI or DVI DDC receiver. This pin will require a pull-up 1.8 kΩ Resistor to +5V
66	In/Out	RESERVED	Reserved Pin. This pin should be floating or pull low with 10 kΩ resistor
67	In	XI	Crystal Input / External Reference Input A parallel resonance crystal should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI Input
68	Out	XO	Crystal Output A parallel resonance crystal should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open
70	Out	DAC2	Analog B Output Full swing is up to 0.7V
72	Out	DAC1	Analog G Output

			Full swing is up to 0.7V
74	Out	DAC0	Analog R Output Full swing is up to 0.7V
76	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2 kΩ, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces
77	Out	GPIO2	General Purpose Output Pin
78	Out	GPIO1	General Purpose Output Pin
80	In/Out	PROM_SD	Serial Port Data to Boot ROM This pin functions as the bi-directional data pin of the serial port to Boot ROM. The pin also can be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level
81	Out	PROM_SC	Serial Port Clock Output to Boot ROM This pin functions as the clock pin of the serial port to Boot ROM. The pin also can be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level
83	In	RSTB	Reset Pin Low for reset
84	In	RESERVED	Reserved Pin This pin should be pull up with 10 kΩ resistor
85	Out	IRQ	Programmed Interrupt Output. Default output 3.3V CMOS level, and this pin could work as open drain structure for other voltages.
86	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up 5.6 kΩ Resistor is required
87	In/Out	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up 5.6 kΩ Resistor is required
88	In	HPD	Hot Plug Detect This input pin determines whether the HDMI output driver is connected to a HDMI monitor.
1,20	Power	AVDD_PLL	PLL Power Supply(1.8V)
4,61	Power	VDDMS	SDRAM Device Power Supply(3.3V)
11,12	Power	VDDH	HDMI Power Supply(3.3V)
19,57	Power	DVDD	Digital Power Supply(1.8V)
23	Power	VDDR	LVDS Input Power Supply (3.3V)
40	Power	VDDT	LVDS Output Power Supply (3.3V)
46,79	Power	AVDD	Analog Power Supply(3.3V)
54,62	Power	VDDMQ	SDRAM Buffer Power Supply(3.3V)
69,73	Power	AVDD_DAC	DAC Power Supply (2.5~3.3V)
2,21	Ground	AGND_PLL	PLL Ground
5,60	Ground	GNDMS	SDRAM Device Ground
6,17	Ground	VSSH	HDMI Ground
18,56	Ground	DGND	Digital Ground

22	Ground	VSSR	LVDS Input Ground
45	Ground	VSST	LVDS Output Ground
50,82	Ground	AGND	Analog Ground
55,63	Ground	GNDMQ	SDRAM Buffer Ground
71,75	Ground	AGND_DAC	DAC Ground
Thermal Exposed Pad	Ground		Connect to ground plane through thermal via

Notes:

1. Default 3.3V CMOS level output.
2. If DDC is not used, both pins DDC_SC/DDC_SD should be connected to ground by 10kΩ resistor.

2.0 PACKAGE DIMENSIONS

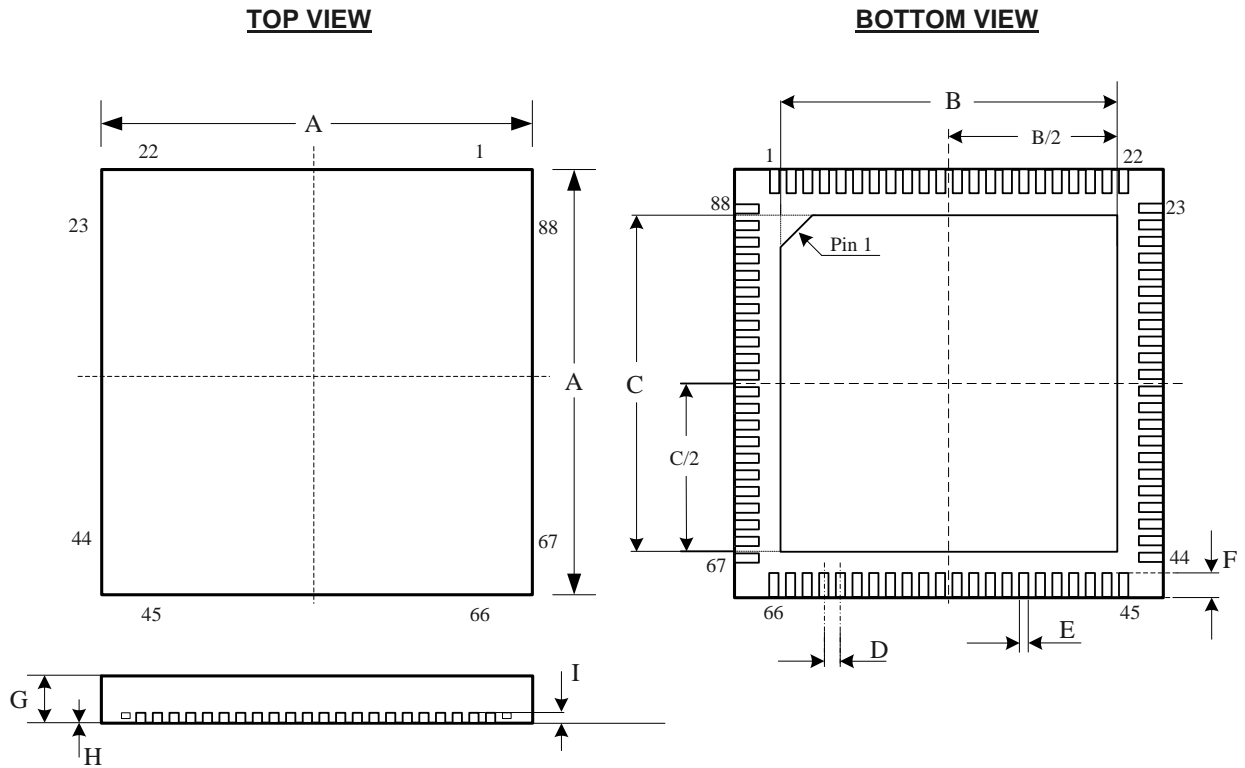


Figure 3: 88 Pin QFN Package (10 x 10 mm)

Table of Dimensions

No. of Leads		SYMBOL								
88 (10 X 10 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	9.90	6.65	6.65	0.30	0.15	0.40	0.80	0	0.20
	NOM	10.00	6.75	6.75	0.40	0.20	0.50	0.85	-	
	MAX	10.10	6.85	6.85	0.50	0.25	0.60	0.90	0.05	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION			
Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7036A-BF	88QFN, Lead-free	Commercial : 0 to 70°C	168/Tray
CH7036A-BFI	88QFN, Lead-free	Industrial: -40 to 85°C	168/Tray

Chrontel

Chrontel International Limited

129 Front Street, 5th floor,
Hamilton, Bermuda HM12
www.chrontel.com
E-mail: sales@chrontel.com