CH7108B HDMI to CVBS/S-Video Converter

FEATURES

- HDMI Receiver compliant with HDMI 1.4 specification
- Support CVBS and S-Video output in format of NTSC or PAL
- On-chip Audio encoder which support 2 channel IIS/ S/PDIF audio output
- MCU embedded to handle the control logic
- Support device boot up by automatically loading firmware from on-chip flash
- Integrated EDID Buffer
- TV connection detection supported
- HDMI input detection supported
- Scaler engine integrated for 640x480 safe mode input supported
- Support Auto Power Saving mode and low stand-by current
- Support RGB to YCC conversion in ITU-R BT.601 and 709 color space
- IIC slave interface and HDMI DDC interface are available for debug and firmware update.
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 40-Pin QFN package (5 x 5 mm)

APPLICATION

- Car Infotainment Device
- HDMI to CVBS/S-Video Adapter/Docking Station
- Notbook/Ultrabook
- Tablet Device
- Handheld/Portable Device
- Digital Video Systems

GENERAL DESCRIPTION

Chrontel's CH7108B is a low-cost, low-power semiconductor device that consists of HDMI receiver, three separate 9-bit video Digital-to-Analog Converters (DACs), SDTV encoder and audio encoder, which can convert HDMI signals into SDTV outputs with IIS or SPDIF audio output.

The HDMI Receiver integrated is compliant with HDMI 1.4b. With sophisticated MCU and the on-chip flash, CH7108B supports auto-boot and EDID buffer. Leveraging the firmware auto loaded from the embedded flash, CH7108B can support HDMI input detection, DAC connection detection and determine to enter into Power saving mode automatically

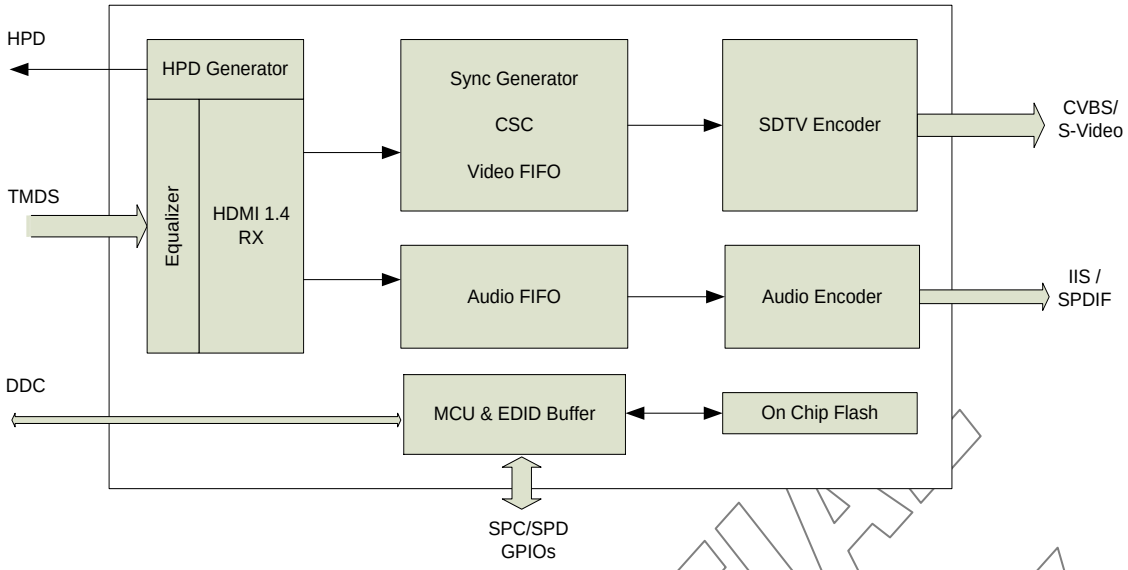

Figure 1: CH7108B Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

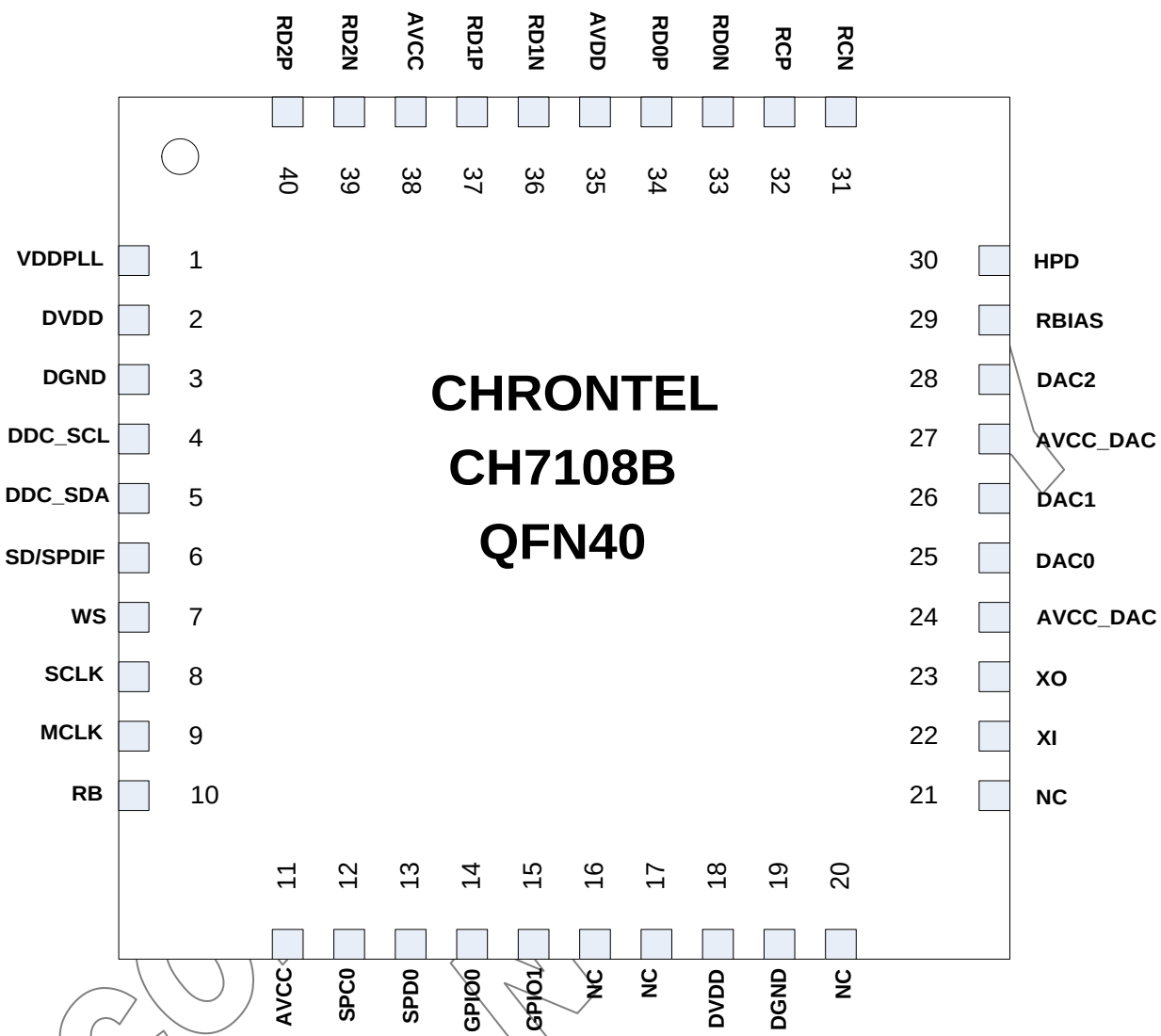

Figure 2: CH7108B 40-Pin QFN Pin Out

1.2 Pin Description

Table 1: Pin Name Descriptions

Pin #	Type	Symbol	Description
4	In	DDC_SCL	**Serial Port Clock to HDMI/DVI Transmitter** This pin functions as the clock bus of the serial port to HDMI or DVI DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level.
5	In/out	DDC_SDA	**Serial Port Data to HDMI/DVI Transmitter** This pin functions as the data bus of the serial port to HDMI or DVI DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level.
6	Out	SD/SPDIF	**I2S Serial Data or SPDIF Output**
7	Out	WS	**I2S Word Select**
8	Out	SCLK	**I2S Continuous Serial Clock**
9	Out	MCLK	**I2S System Clock**
10	In	RB	**Chip Reset** Low to 0V for reset. Typical High level is 3.3V
12	In	SPC0	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
13	In/out	SPD0	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required
14,15	In/Out	GPIO	**General Purpose Input/Output**
16,17,20, 21	NC	NC	**Not Connected**
22	In	XI	**Crystal Input** A parallel resonance crystal should be attached between this pin and XO.
23	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open.
25	Out	DAC0	**SDTV C Component/CVBS DAC output**
26	Out	DAC1	**SDTV Y Component/CVBS DAC output**
28	Out	DAC2	**CVBS DAC output**
29	In	RBIAS	**Current Set Resistor Input** This pin sets the DAC current. A 10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces
30	Out	HPD	**HDMI Receiver Hot Plug output**
31,32,33, 34,36,37, 39,40	In	RD[2:0]P/N RCP/N	**HDMI TMDS Input** HDMI differential clock and data input pairs
1	Power	VDDPLL	**PLL Power Supply (1.2V)**
2,18	Power	DVDD	**Digital IO Power Supply (1.2V)**
3,19	Power	DGND	**Digital Ground**
11, 38	Power	AVCC	**Analog Power Supply (3.3V)**
24,27	Power	AVCC_DAC	**Analog Power Supply (3.3V)**

35	Power	AVDD	**HDMI Receiver Analog Power Supply (1.2V)**
Pad	Power	GND	**Power Supply Ground**

2.0 PACKAGE DIMENSION

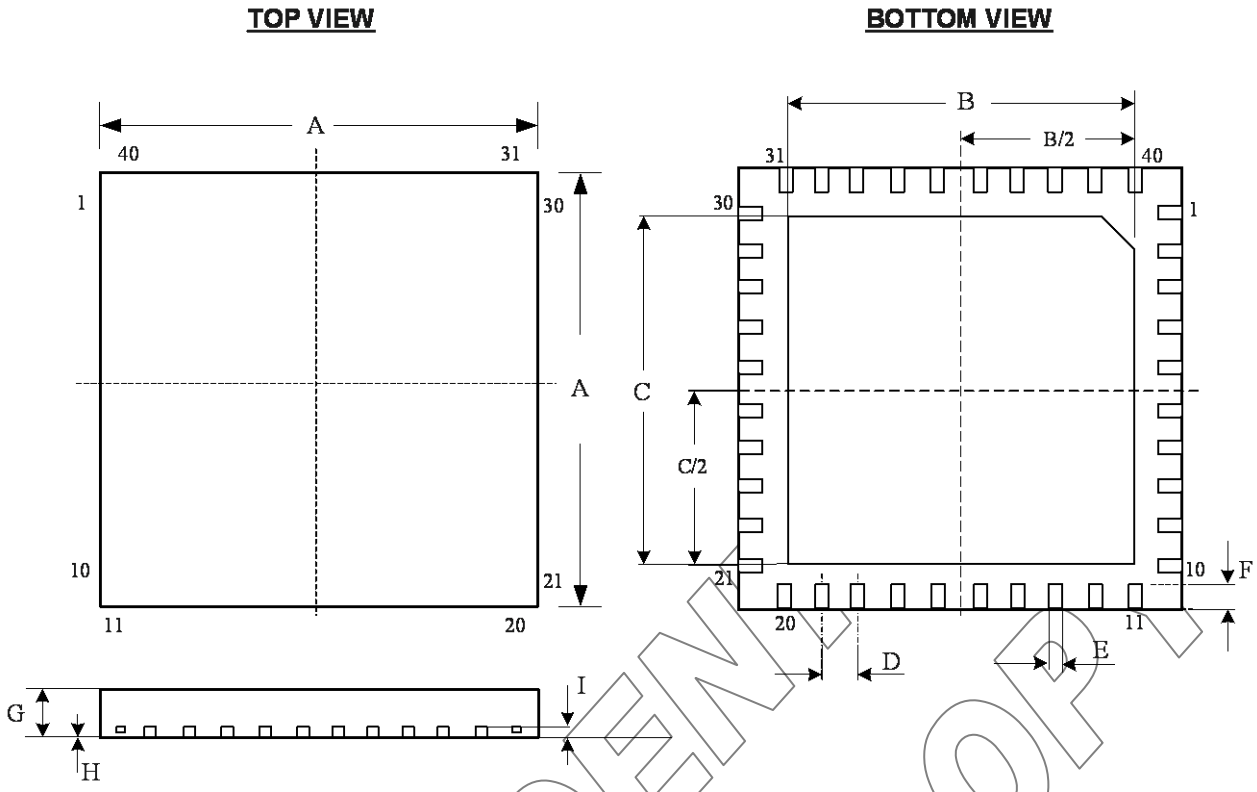

Figure 3: 40 Pin QFN Package

Table of Dimensions

No. of Leads		SYMBOL								
40 (5 X 5 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	4.90	3.20	3.20	0.4	0.15	0.35	0.70	0	0.203 REF
	MAX	5.10	3.40	3.40		0.25	0.45	0.80	0.05	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION

Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7108B-BF	40 QFN, Lead-free	Commercial: 0 to 70°C	490/Tray
CH7108B-BFI	40 QFN, Lead-free	Industrial: -40 to 85°C	490/Tray

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