CH7206A DVD-TV Encoder

FEATURES

- YPrPb support for 480i, 576i, 480p and 576p Output
- Programmable digital input interface supporting RGB and YCrCb input data formats
- Interlaced to progressive scan conversion for DVD
- Support for NTSC, PAL TV and Progressive Scan formats
- Support for SCART output
- TV connection detection
- Outputs of CVBS, S-Video and YPbPr
- Two sets of individual DAC output pins, CVBS, S-Video and YPbPr to allow switching among TV- out connectors without additional external video switches
- Programmable power management
- Four 10-bit video DAC outputs
- Fully programmable through serial port
- Offered in a 48-pin LQFP package

GENERAL DESCRIPTION

The CH7206A is a video TV encoder device for DVD applications which accepts a digital video input signal, encodes and transmits data through four 10-bit high speed DACs. The device is able to generate synchronization signals for NTSC and PAL TV standards with CVBS, S-Video outputs, and YPrPb outputs (480i, 576i, 480p and 576p).

The device accepts data over one 12-bit (or 8-bit) wide data port with dual edge clock data transfer for multiplexed data (24 bit or 16 bit) through variable voltage data port which supports 5 different data formats including RGB and YCrCb.

A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. ITU-R BT.656 interlaced video can be input and scan converted to non-interlaced video.

In addition to TV encoder modes, bypass modes are included which perform color space conversion to HDTV standards and generate and insert HDTV sync signals.

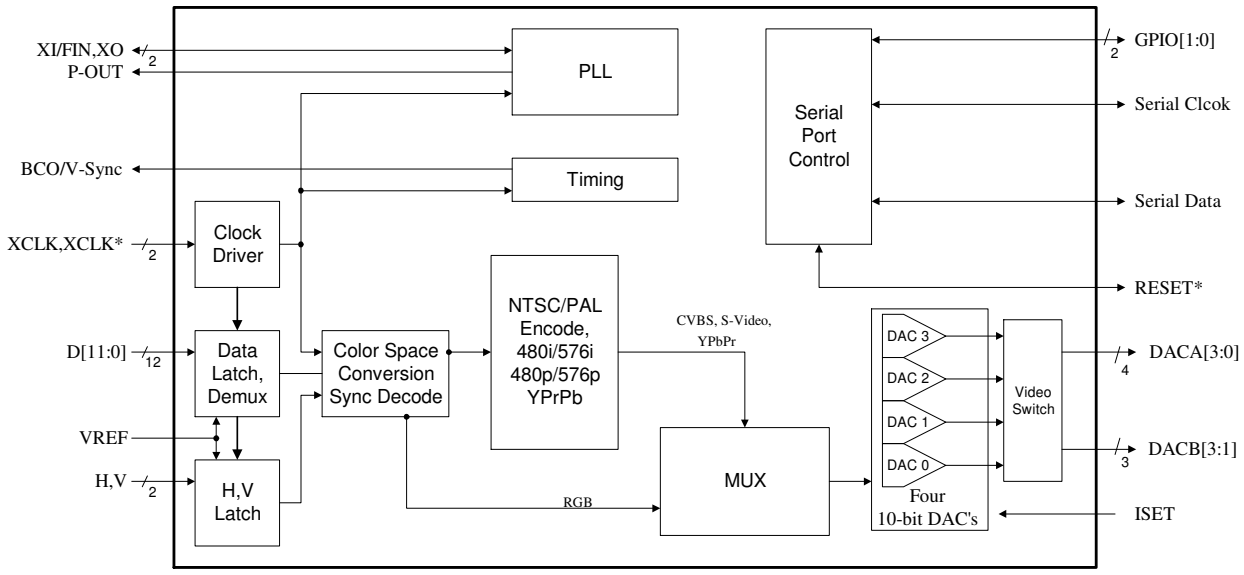

Figure 1: **Functional Block Diagram (CH7206A 48 pin package)**

Table of Contents

Features....1
General Description....1
1.0 Pin-Out....3
1.1 Package Diagram....3
1.2 Pin Description....4
2.0 Functional Description....6
2.1 Modes of Operation....6
2.2 TV Encoder Outputs....8
2.3 Input Interface....8
2.4 TV Output....12
3.0 Register Control....19
3.1 Non-Macrovision Control Registers Index....19
3.2 Non-Macrovision Control Registers Map....21
3.3 Non-Macrovision Control Registers Description....22
4.0 Electrical Specifications....38
4.1 Absolute Maximum Ratings....38
4.2 Recommended Operating Conditions....38
4.3 Electrical Characteristics....39
4.4 Digital Inputs / Outputs....39
4.5 AC Specifications....40
4.6 Timing Information....41
5.0 Package Dimensions....44
6.0 Revision History....45

1.0 PIN-OUT

1.1 Package Diagram

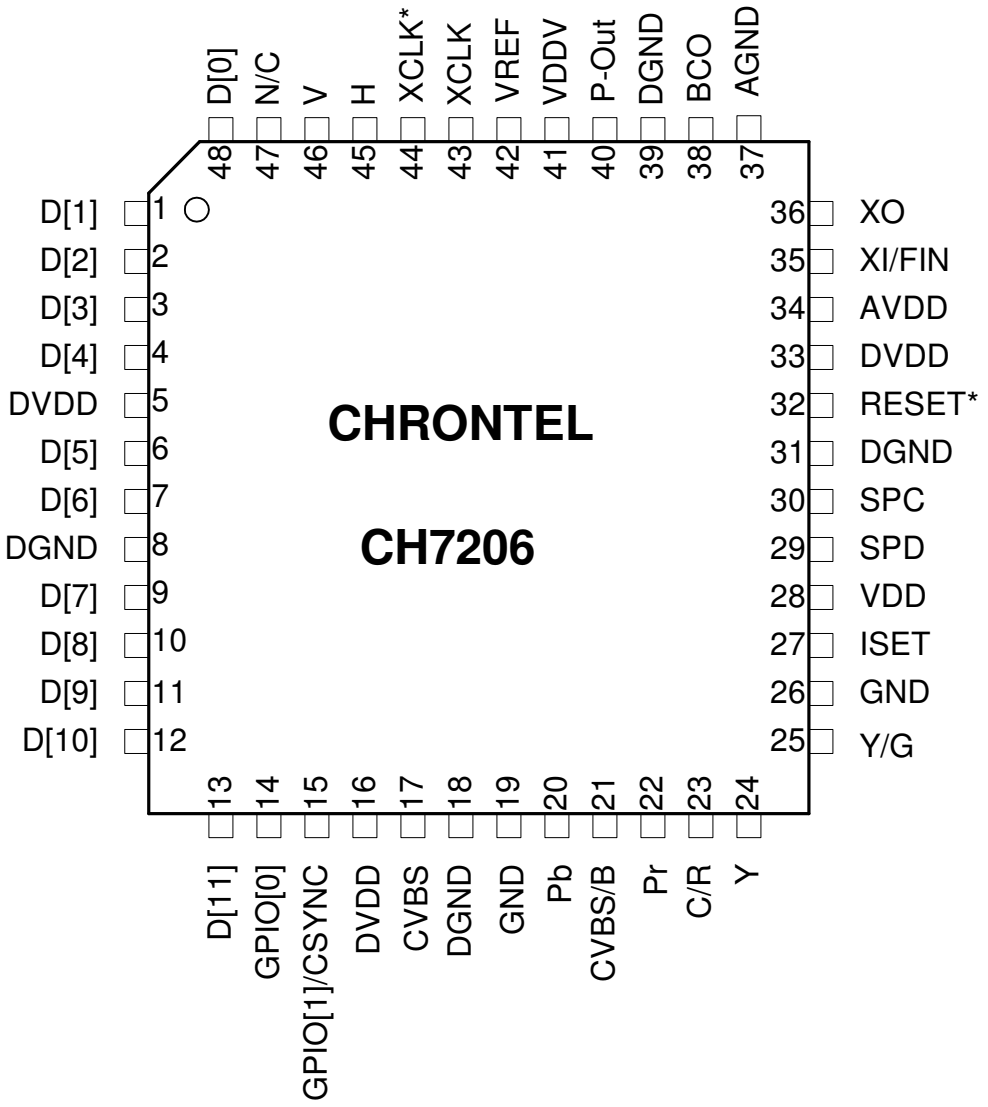

Figure 2: 48-Pin LQFP Package

1.2 Pin Description

Table 1: Pin Description

Pin #	# of Pins	Type	Symbol	Description
1-4, 6,7, 9-13, 48	12	In	D[11]-D[0]	**Data[11] through Data[0] Inputs** These pins accept the 12 data inputs from a digital video port The levels are 0 to VDDV, and the VREF signal is used as the threshold level.
14	1	In/Out	GPIO0	**General Purpose Input – Output0** (weak internal pull-up) This pin provides general purpose I/O controlled via the serial port. This allows an external switch to be used to select NTSC or PAL at power-up. The internal pull-up will be to the DVDD supply.
15	1	In/Out	GPIO1 / CSYNC	**General Purpose Input – Output1** (weak internal pull-up) This pin provides general purpose I/O controlled via the serial port. This allows an external switch to be used to select NTSC or PAL at power-up. The internal pull-up will be to the DVDD supply. It can also be configured to output composite sync.
17	1	Out	CVBS (DAC3)	**Composite Video** This pin outputs a composite video signal capable of driving a 75 ohm doubly terminated load. During bypass modes this output is valid only if the data format is compatible with one of the TV-Out display modes.
20	1	Out	Pb (DACB0)	**Pb Output** This pin outputs the Pb component of YPrPb. The output is designed to drive a 75 ohm doubly terminated load.
21	1	Out	CVBS/B (DACA0)	**Composite Video / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be composite video or blue (for SCART type 1 connections).
22	1	Out	Pr (DACB2)	**Pr Output** This pin outputs the Pr component of YPrPb. The output is designed to drive a 75 ohm doubly terminated load.
23	1	Out	C/R (DACA2)	**Chroma / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video chrominance or red (for SCART type 1 connections).
24	1	Out	Y (DACB1)	**Luma** This pin outputs the luminance component of YPrPb. The output is designed to drive a 75 ohm doubly terminated load.
25	1	Out	Y/G (DACA1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video luminance or green (for SCART type 1 connections).
27	1	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 140 ohm resistor should be connected between this pin and GND (pin 26) using short and wide traces.
29	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to VDDV. Outputs are driven from 0 to VDDV. The serial port address is 76h.
30	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port and operates with inputs from 0 to VDDV.
32	1	In	RESET*	**Reset * Input** (Internal pull-up) When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.

Table 1: Pin Description *(continued)*

Pin #	# of Pins	Type	Symbol	Description
35	1	In	XI / FIN	**Crystal Input / External Reference Input** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI/FIN input.
36	1	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
38	1	Out	BCO	**Buffered Clock Output** This output pin provides selectable buffered clocks to be output, driven by the DVDD supply. The output clock can be selected using the BCO register. The levels are 0 to DVDD.
40	1	Out	P-OUT	**Pixel Clock Output** This pin provides a pixel clock signal to the MPEG decoder device which can be used as a reference frequency. The output is selectable between 1X and 2X of the pixel clock frequency. The output driver is driven from the VDDV supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
42	1	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
43, 44	2	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The clock polarity used can be selected by the MCP control bit.
45	1	In/Out	H	**Horizontal Sync Input / Output** When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDV, and the VREF signal is used as the threshold level. This pin must be used as an input in all bypass modes. When the SYO control bit is high, the device will output a horizontal sync pulse, 64 pixels wide. The output is driven from the DVDD supply. This output is valid with TV-Out operation.
46	1	In/Out	V	**Vertical Sync Input / Output** When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDV, and the VREF signal is used as the threshold level. This pin must be used as an input in all bypass modes. When the SYO control bit is high, the device will output a vertical sync pulse one line wide. The output is driven from the DVDD supply. This output is valid with TV-Out operation.
5,16,33	3	Power	DVDD	**Digital Supply Voltage** (3.3V)
8,18,31,39	4	Power	DGND	**Digital Ground**
41	1	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
34	1	Power	AVDD	**PLL Supply Voltage** (3.3V)
37	1	Power	AGND	**PLL Ground**
28	1	Power	VDD	**DAC Supply Voltage** (3.3V)
19,26	2	Power	GND	**DAC Ground**

2.0 FUNCTIONAL DESCRIPTION

2.1 Modes of Operation

The CH7206A is capable of being operated as an ITU-R BT.601/656 encoder (with or without a de-interlaced function), or in one of several bypass modes for driving monitors requiring component video signals (Progressive Scan TV, SCART, etc.). All modes make use of the same set of DACs, and therefore cannot be used simultaneously. Table 2 describes the possible operating modes. An 'i' following a number in the Input Scan Type column indicates an interlaced input where the number indicates the active number of lines per frame. Detailed descriptions of each of the operating modes follows Table 2.

Table 2: Operating Modes

Input Scan Type	Input Data Format	Output scan Type	Output Format	Operating Mode	Described In section
interlaced (480i, 576i)	RGB / YCrCb	Non-interlaced	YPbPr	ITU-R BT.601/656 TV Deinterlace (480p, 576p generation)	2.1.2
interlaced (480i, 576i)	RGB / YCrCb	Interlaced	YPbPr	ITU-R BT.601/656 TV Interlace (480i, 576i generation)	2.1.1
interlaced (480i, 576i)	RGB / YCrCb	Interlaced	CVBS, S-Video	ITU-R BT.601/656 TV Encoder (NTSC / PAL)	2.1.1
interlaced (480i, 576i)	RGB / YCrCb	Interlaced	CVBS, RGB	ITU-R BT.601/656 TV Encoder (SCART format)	2.1.1

2.1.1 ITU-R BT.601/656 TV Encoder

In ITU-R BT.601/656 TV Encoder mode, interlaced data, sync and clock signals are input to the CH7206A from the output of an MPEG decoder device. The YCrCb data format is most commonly used in these modes, but RGB data can be used as well. A clock signal (P-OUT) from CH7206A can be output as a frequency reference to the MPEG decoder. Horizontal and vertical sync signals are normally sent to the CH7206A from the MPEG decoder, but can be embedded into the data stream in YCrCb input data formats, or can be output to the MPEG decoder controller. Data is 2X multiplexed, and the XCLK clock signal is 2X times the pixel rate. The input data is encoded into the selected video standard and output from the video DACs. NTSC and PAL formats are supported. CH7206A can output data in S-Video and CVBS format, or as RGB for interface to a SCART connector. The operating resolutions supported for ITU-R BT.601/656 TV output are shown in Table 3 below. The timing of the sync signals is shown in Figure 3 below. Note that the alignment of the VSYNC signal to the HSYNC signal changes from field 1 to field 2 to allow the CH7206A to identify the correct field.

Table 3: ITU-R BT.601/656 TV Encoder Operating Modes

Input Resolution	Active Video Aspect Ratio	Pixel Aspect Ratio	TV Output Standard	Scaling Ratios
720x480i	4:3	9:8	NTSC	1/1
720x576i	4:3	15:12	PAL	1/1

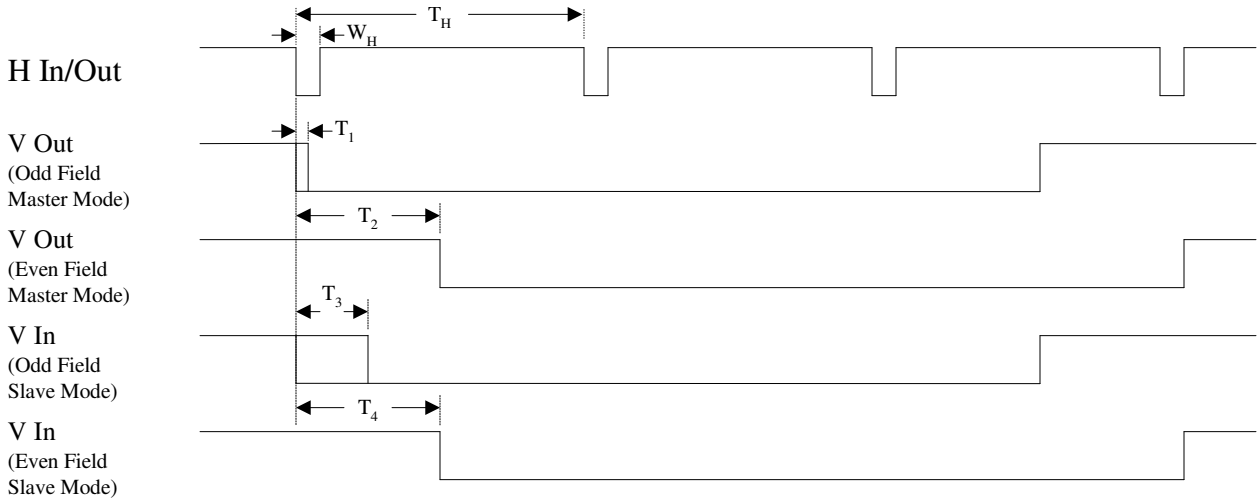

Figure 3: Interlaced Sync Input/Output Timing

Table 4: Interlaced Sync Input/Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_{PCK}	Input clock period	6.73		47.62	uS
T_H	Total Line Period				
	SDTV	63.5		63.5	uS
	HDTV	14.8		37.0	uS
W_H	Hsync Width				
	When output from CH7206A	64		64	Pixel clocks
	When input to CH7206A	1			Pixel clocks
T_1	Odd Field (Field 1) V SYNC out to H SYNC out alignment		0		uS
T_2	Even Field (Field 2) V SYNC out delay from H SYNC out		$0.5*T_H$		uS
T_3	Odd Field (Field 1) V SYNC in to H SYNC in alignment	0		$W_H - T_{PCK}$	uS
T_4	Even Field (Field 2) V SYNC in delay from H SYNC in	W_H		$T_H - T_{PCK}$	uS

2.1.2 ITU-R BT.601/656 TV De-Interlace

In ITU-R BT.601/656 TV De-Interlace mode, interlaced data, sync and clock signals are input to the CH7206A from the output of an MPEG decoder device. The YCrCb data format is most commonly used as input in De-Interlace modes, but RGB data can be used as well. A clock signal (P-Out) can be output as a frequency reference to the MPEG decoder device. Horizontal and vertical sync signals are normally sent to the CH7206A from the MPEG decoder, but can be embedded into the data stream in YCrCb input data formats, or can be output to the MPEG decoder controller. Data is 2X multiplexed, and the XCLK clock signal is 2X times the pixel rate. Input data is scan converted from interlaced to non-interlaced data, color space converted to the selected video format, has sync signals generated and is output from the video DACs. The output format is YPbPr. The operating resolutions supported for ITU-R BT.601/656 TV De-Interlace mode are shown in Table 5 below. The timing of the sync signals is shown in Figure 3 above. Note that the alignment of the VSYNC signal to the HSYNC signal changes from field 1 to field 2 to allow the CH7206A to identify the correct field.

Table 5: ITU-R BT.601/656 TV De-Interlace Operating Modes

Input Resolution	Active Video Aspect Ratio	Pixel Aspect Ratio	TV Output Standard
720x480i	4:3	9:8	720x480p
720x576i	4:3	15:12	720x576p

2.2 TV Encoder Outputs

In CH7206A, three of the four TV encoder DAC outputs can be switched to two sets of output pins DACA[2:0] and DACB[2:0] via video switches. The fourth DAC output, DACA0 is not switched so that CVBS output is available for the progressive scan TV configuration in addition to the standard TV output configurations. This feature facilitates simple connection to two sets of video connectors as listed in Table 6.

Table 6: TV Output Configurations

CH7206A	2 RCA + 1 S-Video	SCART
DACA0 (pin 21)	CVBS	B
DACA1 (pin 25)	Y	G
DACA2 (pin 23)	C	R
DAC3 (pin 17)	CVBS	CVBS
	SDTV	
DACB0 (pin 20)	Pb	
DACB1 (pin 24)	Y	
DACB2 (pin 22)	Pr	
DAC3 (pin 17)	CVBS	

If the application calls for CVBS/S-video, SCART, and YPrPb to output on one set of DAC output pins, different reconstruction filters for each type of signal can be implemented on the break-out cables.

The CH7206A supports YPrPb output for driving 480i, 480p, 576i and 576p, and SCART TV sets.

Note: CVBS is available with YPrPb for SDTV interlaced outputs.

2.3 Input Interface

2.3.1 Overview

Two distinct methods of transferring data to the CH7206A are described. They are:

- Multiplexed data, clock input at 1X the pixel rate
- Multiplexed data, clock input at 2X the pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7206A is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X pixel rate the data applied to the CH7206A is latched with one edge of the clock (also known as single edge transfer mode or SDR). The polarity of the pixel clock can be reversed under serial port control. In single edge transfer modes, the clock edge used to latch data is programmable. In dual edge transfer modes, the clock edge used to latch the first half of each pixel is programmable.

2.3.2 Input Clock and Data Timing Diagram

Figure 4 below shows the timing diagram for input data and clocks. The first XCLK/XCLK* waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK/XCLK* waveform represents the input clock for the dual edge transfer (DDR) method. The timing requirements are given in section 4.5.

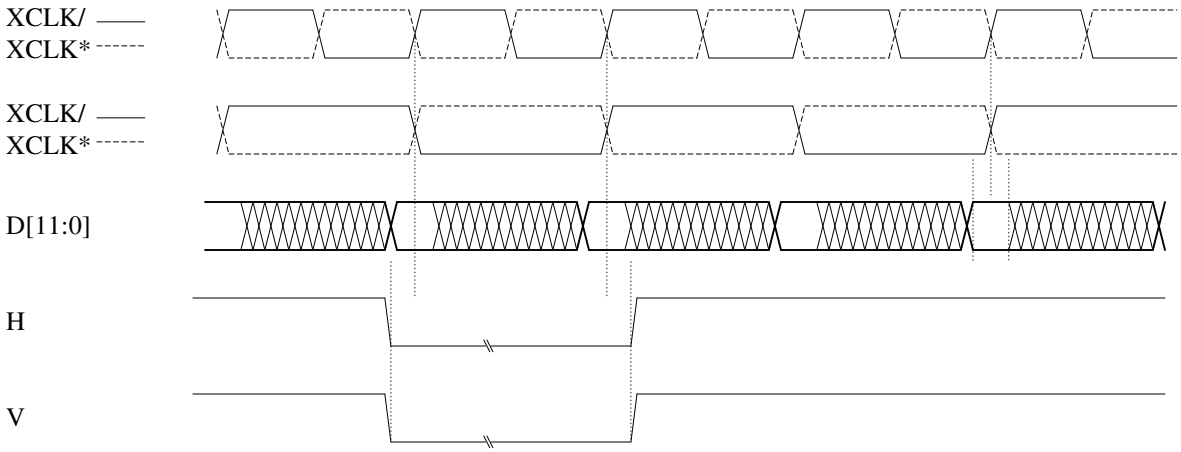

Figure 4: Clock, Data and Interface Timing

2.3.3 Data De-skew Feature

The de-skew feature allows adjustment of the input setup and hold time. The input data D[11:0] can be latched slightly before or after the latching edge of XCLK depending on the amount of the de-skew. Note that the XCLK is not changed, only the time at which the data is latch relative to XCLK. The de-skew is controlled using the XCMD[3:0] bits located in register 1Dh. The delay t_{CD} between clock and data is given by the following formula:

t_{CD} = - XCMD[3:0] * t_{STEP} for $0 \le$ XCMD[3:0] ≤ 7
t_{CD} = (XCMD[3:0] – 8) * t_{STEP} for $8 \le$ XCMD[3:0] ≤ 15

where XCMD is a number between 0 and 15 represented as a binary code
t_{STEP} is the adjustment increment (see section 4.5)

The delay is also tabulated in Table 23.

2.3.4 Input Data Formats

The CH7206A supports 5 different multiplexed data formats, each of which can be used with a 1X clock latching data on both clock edges, or a 2X clock latching data with a single edge (rising or falling depending on the value of the MCP bit – rising refers to a rising edge on the XCLK signal, a falling edge on the XCLK* signal). The input data formats are (IDF[2:0]) as follows:

IDF	Description
0	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 1)
1	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 2)
2	8-bit multiplexed RGB input (16-bit color, 565)
3	8-bit multiplexed RGB input (15-bit color, 555)
4	8-bit multiplexed YCrCb input (24-bit color), (Y, Cr and Cb are multiplexed)

The input data formats are shown in Figure 5 below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.; P0a and P0b) will contain a complete pixel encoded as shown in Table 7 through Table 10.

It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

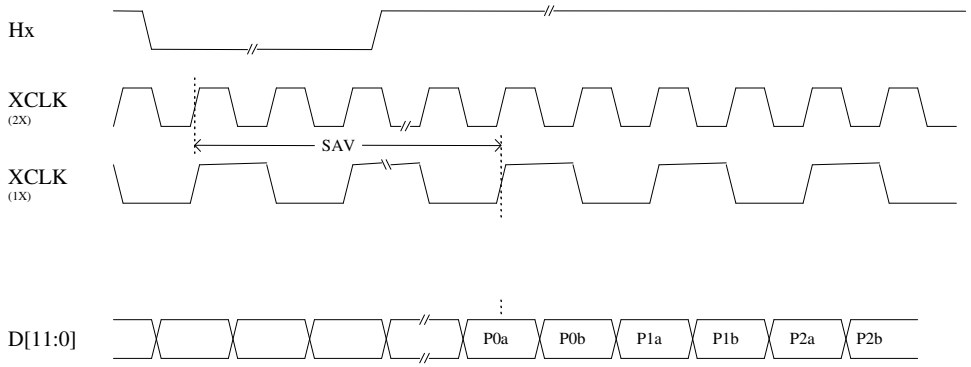

Figure 5: 12-bit Multiplexed Input Data Formats (IDFx = 0,1,2,3,4)

Table 7: Multiplexed Input Data Formats (IDF = 0, 1)

IDF = Format =		0 12-bit RGB				1 12-bit RGB			
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P0a**	**P0b**	**P1a**	**P1b**
Bus Data	D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	D[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 8: Multiplexed Input Data Formats (IDF = 2, 3)

IDF = Format =		2 RGB 5-6-5				3 RGB 5-5-5			
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P0a**	**P0b**	**P1a**	**P1b**
Bus Data	D[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	D[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	D[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	D[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	D[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	D[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	D[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	D[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 9: Multiplexed Input Data Formats (IDF = 4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P2a**	**P2b**	**P3a**	**P3b**
Bus Data	D[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

Table 10: Embedded Sync in Multiplexed Data Format (IDF=4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P2a**	**P2b**	**P3a**	**P3b**
Bus Data	D[7]	1	0	0	S[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	1	0	0	S[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	1	0	0	S[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	1	0	0	S[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	1	0	0	S[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	1	0	0	S[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	1	0	0	S[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	1	0	0	S[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

In this mode, the S[7:0] byte contains the following data:

S[6] = F = 1 during field 2, 0 during field 1

S[5] = V = 1 during field (frame) blank, 0 elsewhere

S[4] = H = 1 during EAV (synchronization reference at the end of active video)
0 during SAV (synchronization reference at the start of active video)

Bits S[7] and S[3:0] are ignored.

2.4 TV Output

2.4.1 Color-Burst Generation

The CH7206A allows the subcarrier frequency to be accurately generated from a 14.31818 MHz crystal oscillator, leaving the subcarrier frequency independent of the graphics pixel clock frequency. This feature is important since even a ±0.01% subcarrier frequency variation is enough to cause some televisions to lose color lock.

In addition, the CH7206A has the capability to genlock the color burst signal to the VGA horizontal sync frequency, which enables a fully synchronous system between the MPEG decoder device and the television. When genlocked, the CH7206A can stop "dot crawl" motion (for composite NTSC modes), thus eliminating the annoyance of moving borders. Both of these features are under programmable control through the register set.

2.4.2 NTSC and PAL Operation

Composite and S-Video outputs are supported in either NTSC or PAL format. The general parameters used to characterize these outputs are listed in Table 11 and shown in Figure 6 (see Figure 7 through Figure 14 for illustrations of composite and S-Video output waveforms).

ITU-R BT.470 Compliance

The CH7206A is predominantly compliant with the recommendations called out in ITU-R BT.470. The following are the only exceptions to this compliance:

- The frequencies of Fsc, Fh, and Fv can only be guaranteed in clock/sync master mode, not in clock/sync slave mode when the graphics device generates these frequencies.
- It is assumed that gamma correction, if required, is performed in the graphics device which establishes the color reference signals.
- All modes provide the exact number of lines called out for NTSC and PAL modes respectively.
- Chroma signal frequency response will fall within 10% of the exact recommended value.
- Pulse widths and rise/fall times for sync pulses, front/back porches, and equalizing pulses are designed to approximate ITU-R BT.470 requirements, but will fall into a range of values due to the variety of clock frequencies used to support multiple operating modes.

In order to minimize the hazard of ESD, a set of protection diodes MUST BE used for each DAC connecting to TV (Refer to AN-38 for details).

Table 11: NTSC/PAL Composite Output Timing Parameters

Symbol	Description	Level (mV)		Duration (us)	
		NTSC	PAL	NTSC	PAL
A	Front Porch	287	300	1.49 - 1.51	1.48 - 1.51
B	Horizontal Sync	0	0	4.69 - 4.72	4.69 - 4.71
C	Breezeway	287	300	0.59 - 0.61	0.88 - 0.92
D	Color Burst	287	300	2.50 - 2.53	2.24 - 2.26
E	Back Porch	287	300	1.55 - 1.61	2.62 - 2.71
F	Black	340	300	0.00 - 7.50	0.00 - 8.67
G	Active Video	340	300	37.66 - 52.67	34.68 - 52.01
H	Black	340	300	0.00 - 7.50	0.00 - 8.67

For this table and all subsequent figures, key values are:

Note:

1. R(ISET) = 140 ohms; V(ISET) = 1.235V; 75 ohms doubly terminated load. R(ISET) is the resistor connected to the pin ISET.
2. Durations vary slightly in different modes due to the different clock frequencies used.
3. Active video and black (F, G, H) times vary greatly due to different scaling ratios used in different modes.
4. Black times (F and H) vary with position controls.

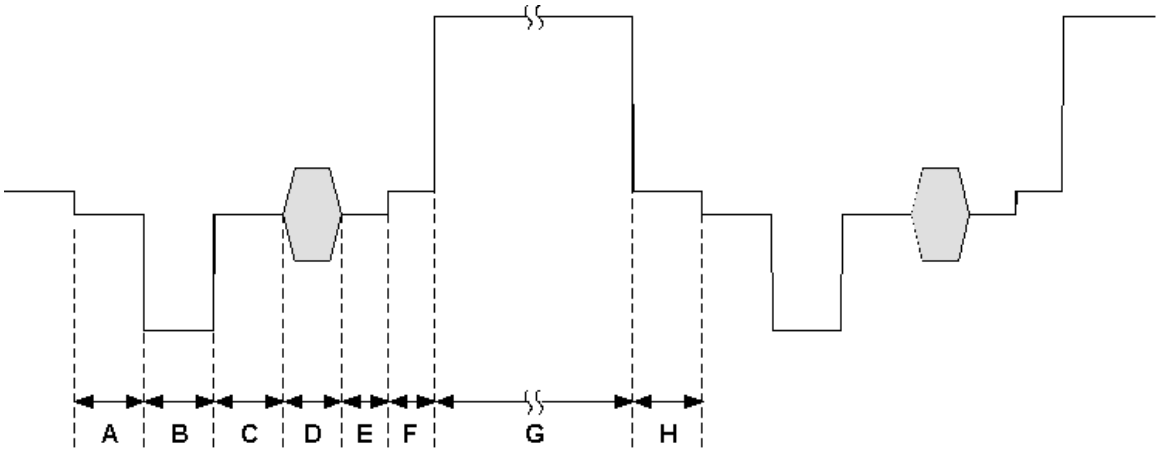

Figure 6: NTSC / PAL Composite Output

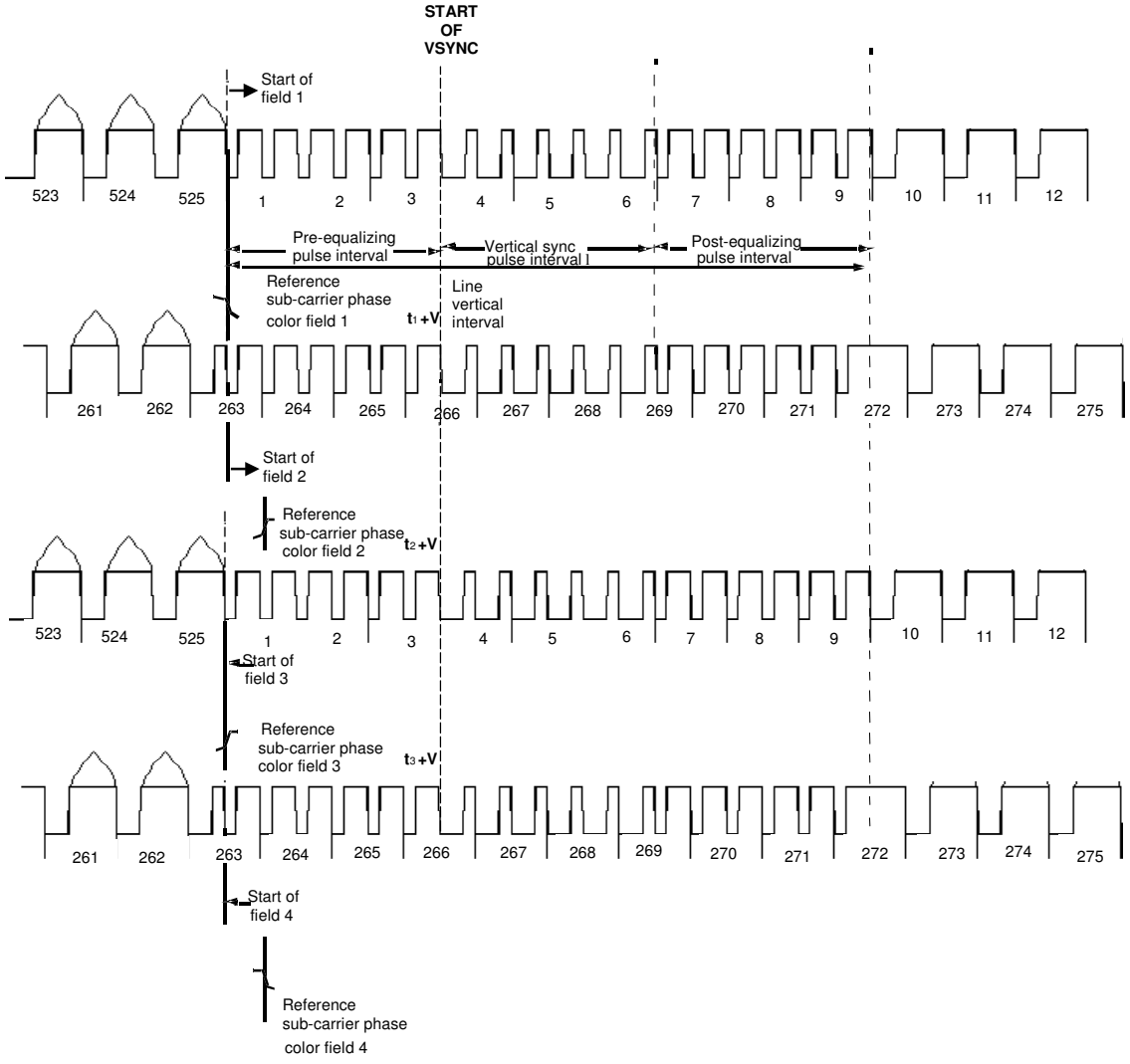

Figure 7: **Interlaced NTSC Video Timing**

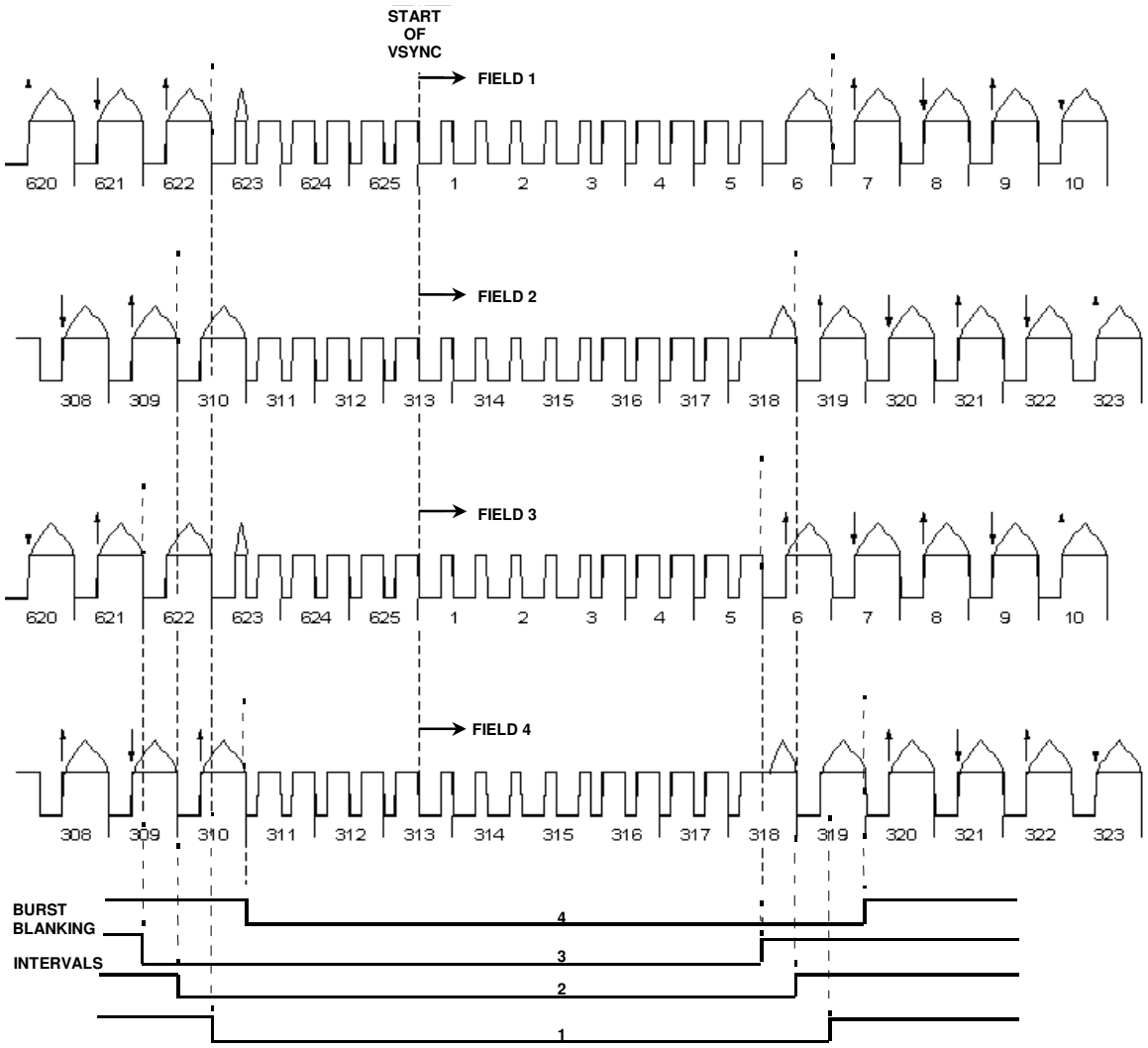

Figure 8: **Interlaced PAL Video Timing**

Color/Level	mA	V
White	26.66	1.000
Yellow	24.66	0.925
Cyan	21.37	0.801
Green	19.37	0.726
Magenta	16.22	0.608
Red	14.22	0.533
Blue	11.08	0.415
Black	9.08	0.340
Blank	7.65	0.287
Sync	0.00	0.000

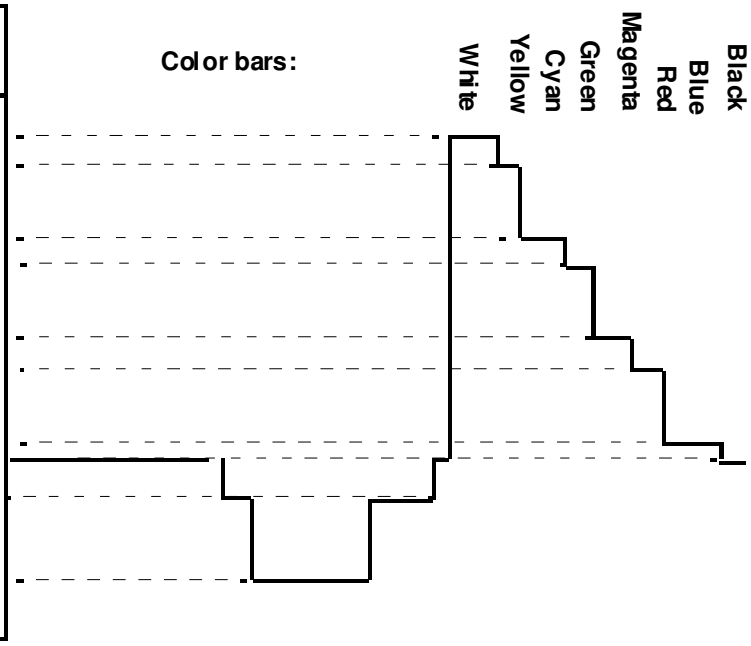

Figure 9: **NTSC Y (Luminance) Output Waveform (DACG = 0)**

Color/Level	mA	V
White	26.75	1.003
Yellow	24.62	0.923
Cyan	21.11	0.792
Green	18.98	0.712
Magenta	15.62	0.586
Red	13.49	0.506
Blue	10.14	0.380
Blank/ Black	8.00	0.300
Sync	0.00	0.000

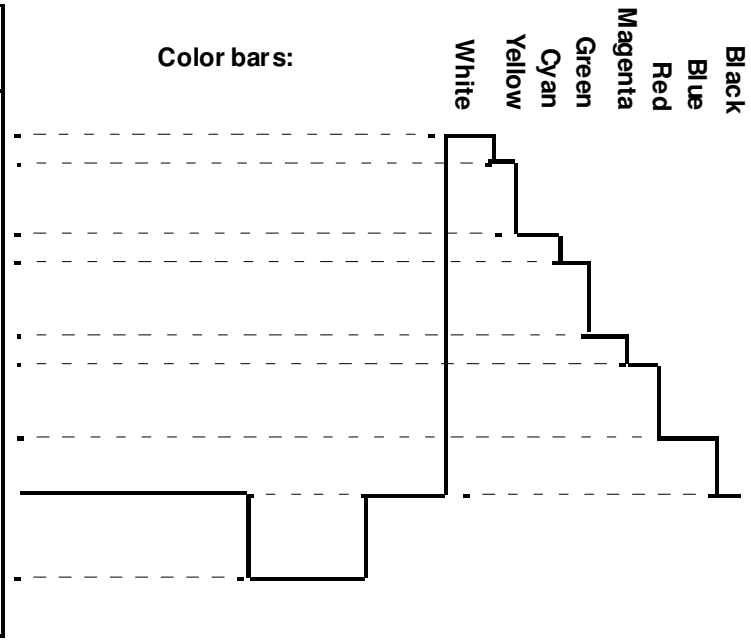

Figure 10: **PAL Y (Luminance) Video Output Waveform (DACG = 1)**

Color/Level	mA	V
Cyan/Red	25.80	0.968
Green/Magenta	25.01	0.938
Yellow/Blue	22.44	0.842
Peak Burst	18.08	0.678
Blank	14.29	0.536
Peak Burst	10.51	0.394
Yellow/Blue	6.15	0.230
Green/Magenta	3.57	0.134
Cyan/Red	2.79	0.105

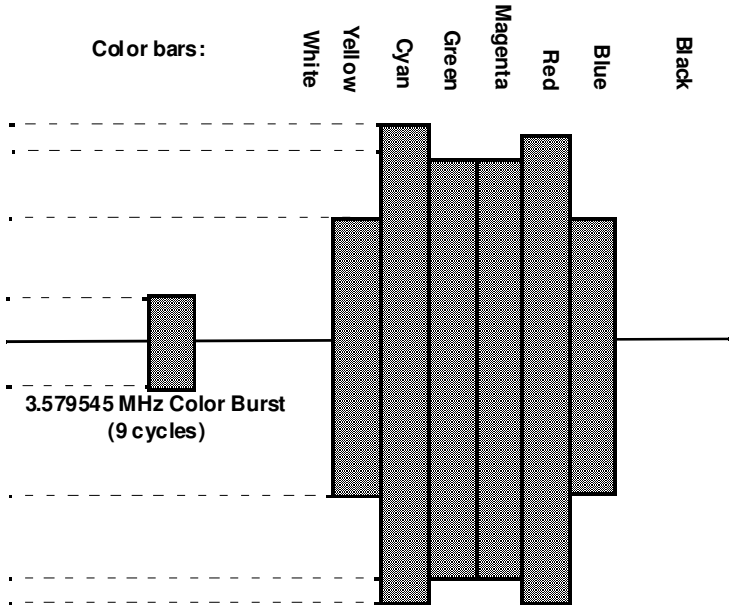

Figure 11: **NTSC C (Chrominance) Video Output Waveform (DACG = 0)**

Color/Level	mA	V
Cyan/Red	27.51	1.032
Green/Magenta	26.68	1.000
Yellow/Blue	23.93	0.897
Peak Burst	19.21	0.720
Blank	15.24	0.572
Peak Burst	11.28	0.423
Yellow/Blue	6.56	0.246
Green/Magenta	3.81	0.143
Cyan/Red	2.97	0.111

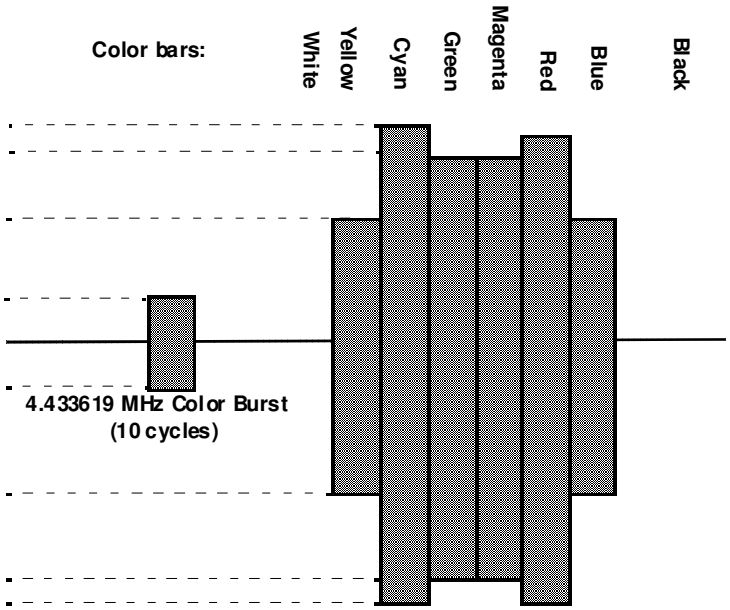

Figure 12: **PAL C (Chrominance) Video Output Waveform (DACG = 1)**

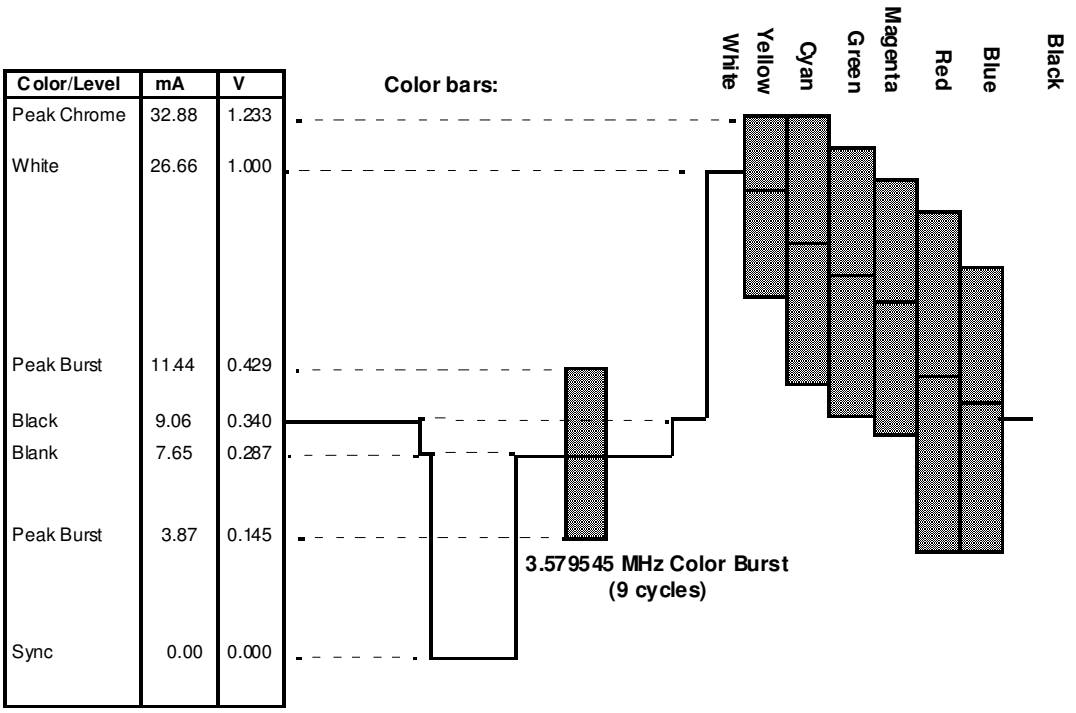

Figure 13: Composite NTSC Video Output Waveform (DACG = 0)

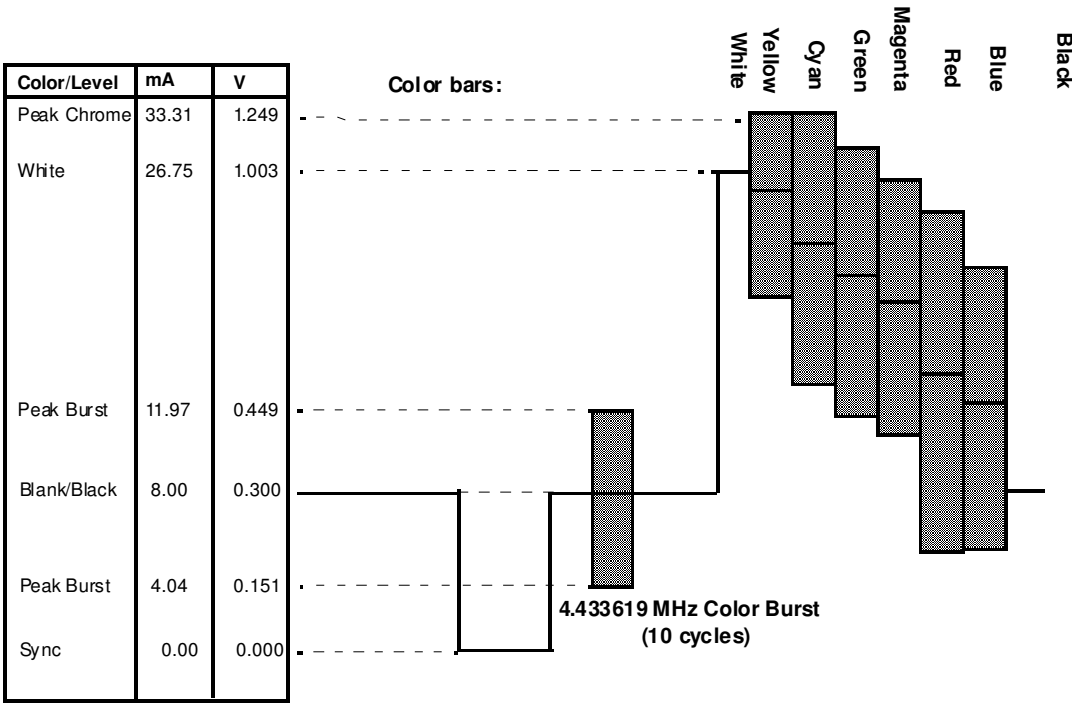

Figure 14: Composite PAL Video Output Waveform (DACG = 1)

3.0 REGISTER CONTROL

The CH7206A is controlled via a serial control port. The serial bus uses only the SC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device should retain all register values during power down modes.

Regarding the CH7206A registers read/write operation, please see Application Note AN-41 for details.

3.1 Non-Macrovision Control Registers Index

The non-Macrovision controls are listed below, divided into three sections: General & Power Down controls, Input/Output controls, TV-Out controls.

Table 12: Control Register Index

Name	Description	Address
GENERAL & POWER DOWN CONTROLS		
DACPD[3:0]	DAC Power Down	49h
DID[7:0]	Device ID register	4Bh
ResetIB	Software SPP (serial port) reset	48h
ResetDB	Software datapath reset	48h
TSTP[1:0]	Enable/select test pattern generation (color bar, ramp)	48h
TVPD	TV power down	49h
VID[7:0]	Version ID register	4Ah
INPUT/OUTPUT CONTROLS		
BCO[2:0]	Select output signal for BCO pin	22h
BCOEN	Enable BCO Output	22h
BCOP	BCO polarity	22h
BGBST	Bandgap Boost	14h
DACBP	DAC bypass	21h
DACG[1:0]	DAC gain control	21h
DACT[3:0]	DAC termination sense	20h
DES	Decode embedded sync	1Fh
GOENB[1:0]	Direction control for GPIO pins	1Eh
GPHSS	General Purpose / Horizontal Sync Select	48h
GPIOL[1:0]	Read or Write Data for GPIO pins	1Eh
HSP	H sync polarity control	1Fh
IBS	Input buffer type select for D[11:0]	1Fh
IDF[2:0]	Input Data Format for D[11:0]	1Fh
MCP	XCLK Polarity Control for D[11:0]	1Ch
PCM	P-Out 1X, 2X select	1Ch
POUTE	P-Out enable	1Eh
POUTP	P-Out clock polarity	1Eh
SENSE	TV Sense	20h
SICN	Serial Port N Enable	10h
SICP	Serial Port P Enable	10h
SYNCO[1:0]	Select Sync output on GPIO1	21h
SYO	H/V sync direction control	1Fh
VSP	V sync polarity control for	1Fh
XCM	XCLK 1X / 2X select for D[11:0]	1Ch
XCMD[3:0]	Delay adjust between XCLK and D[11:0]	1Dh
XOSC[2:0]	Crystal oscillator adjustments	21h, 20h

TV-OUT CONTROLS		
BL[7:0]	TV-Out Black level control	07h
BLKEN	Black Level control register update	1Dh
CBW	Chroma video bandwidth	02h
CE[2:0]	TV-Out contrast enhancement	08h
CFRB	Chroma sub-carrier free run (bar) control	02h
CIV[25:0]	Calculated sub-carrier increment value read out	10h-13h
CIVC[1:0]	Calculated sub-carrier control (hysteresis)	10h
CIVEN	Calculated sub-carrier enable	10h
CVBWB	CVBS DAC receives black & white (S-Video) signal	02h
FSCI[32:0]	Sub-carrier generation increment value (when ACIV=0)	0Ch-0Fh
HDTV	Enable HDTV modes	14h
HP[8:0]	TV-Out horizontal position control	05h, 03h
IR[2:0]	Input data resolution	00h
M/S*	TV-Out PLL reference input control	1Ch
M[8:0]	TV-Out PLL M divider	0Ah, 09h
MEM[2:0]	Memory sense amp reference adjust	09h
N[9:0]	TV-Out PLL N divider	0Bh, 09h
PALN	Select PAL-N when in a CIV mode	10h
PEDL[7:0]	Pedestal level register	4Fh
PLLCAP	TV-Out PLL Capacitor Control	09h
PLLCPI	TV-Out PLL Charge Pump control settings	09h
SAV[8:0]	Horizontal start of active video	04h, 03h
VBID	Vertical blanking interval defeat	02h
VOF[1:0]	TV-Out video format (s-video & composite, YPrPb or RGB)	01h
VOS[1:0]	TV-Out video standard	00h
VP[8:0]	TV-Out vertical position control	06h, 03h
YCV[1:0]	Composite video luma bandwidth	02h
YSV[1:0]	S-Video luma bandwidth	02h

3.2 Non-Macrovision Control Registers Map

Table 13: Non-Macrovision Serial Port Register Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	IR2	IR1	IR0	VOS1	VOS0	Reserved	Reserved	Reserved
01h	VOF1	VOF0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
02h	VBID	CFRB	CVBWB	CBW	YSV1	YSV0	YCV1	YCV0
03h	Reserved	Reserved	SAV8	HP8	VP8	Reserved	Reserved	Reserved
04h	SAV7	SAV6	SAV5	SAV4	SAV3	SAV2	SAV1	SAV0
05h	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
06h	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
07h	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
08h	Reserved	Reserved	Reserved	Reserved	Reserved	CE2	CE1	CE0
09h	MEM2	MEM1	MEM0	N9	N8	M8	PLLCPI	PLLCAP
0Ah	M7	M6	M5	M4	M3	M2	M1	M0
0Bh	N7	N6	N5	N4	N3	N2	N1	N0
0Ch	FSCI31	FSCI30	FSCI29	FSCI28	FSCI27	FSCI26	FSCI25	FSCI24
0Dh	FSCI23	FSCI22	FSCI21	FSCI20	FSCI19	FSCI18	FSCI17	FSCI16
0Eh	FSCI15	FSCI14	FSCI13	FSCI12	FSCI11	FSCI10	FSCI9	FSCI8
0Fh	FSCI7	FSCI6	FSCI5	FSCI4	FSCI3	FSCI2	FSCI1	FSCI0
10h	SICP	SICN	CIV25	CIV24	CIVC1	CIVC0	PALN	CIVEN
11h	CIV23	CIV22	CIV21	CIV20	CIV19	CIV18	CIV17	CIV16
12h	CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8
13h	CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0
14h	BGBST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HDTV
1Ch	Reserved	Reserved	Reserved	Reserved	M/S*	MCP	PCM	XCM
1Dh	Reserved	BLKEN	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
1Eh	GOENB1	GOENB0	GPIOL1	GPIOL0	Reserved	Reserved	POUTE	POUTP
1Fh	IBS	DES	SYO	VSP	HSP	IDF2	IDF1	IDF0
20h	Reserved	XOSC2	Reserved	DACT3	DACT2	DACT1	DACT0	SENSE
21h	XOSC1	XOSC0	Reserved	SYNCO1	SYNCO0	DACG1	DACG0	DACBP
22h	Reserved	Reserved	Reserved	BCOEN	BCOP	BCO2	BCO1	BCO0
48h	GPHSS	VSGLN	Reserved	ResetIB	ResetDB	Reserved	TSTP1	TSTP0
49h	Reserved	Reserved	Reserved	DACPD3	DACPD2	DACPD1	DACPD0	TVPD
4Ah	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
4Bh	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
4Fh	PEDL7	PEDL6	PEDL5	PEDL4	PEDL3	PEDL2	PEDL1	PEDL0

3.3 Non-Macrovision Control Registers Description

Display Mode Register

Symbol: **DM**
Address: **00h**
Bits: **5**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	IR2	IR1	IR0	VOS1	VOS0	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	1	0	0	0

Register DM provides programmable control of the CH7206A TV display modes, including input resolution (IR[2:0]), video output standard (VOS[1:0]). The mode of operation is determined according to Table 14 below when the HDTV bit (register 14h, bit 0) = '1'. These are the HDTV modes. When HDTV bit (register 03h, bit 7) = '0' the mode of operation is determined according to Table 16 below. These are the SDTV modes. For entries in which the output standard is shown as PAL, PAL-B,D,G,H,I,N,N_C can be supported through proper selection of the chroma sub-carrier. For entries in which the output standard is shown as NTSC, NTSC-M,J and PAL-M can be supported through proper selection of VOS[1:0] and chroma sub-carrier.

Table 14: Display Mode for Standard TV (HDTV = '0')

Mode	IR[2:0]	VOS [1:0]	Input Data Format (Active Video)	Total Pixels/Line x Total Lines/Frame	Output Standard [TV Standard]	Percent Overscan	Pixel Clock (MHz)
37[1]	101	00	720x576	864x625	PAL	0	13.500000
38[1]	100	01	720x480	858x525	NTSC	0	13.500000

[1] These DVD modes operate with interlaced input.

Table 15: Video Output Standard Selection (HDTV = '0')

VOS[1:0]	00	01	10	11
Output Format	PAL	NTSC	PAL-M	NTSC-J

The mode of operation is determined according to Table 16 below when the HDTV bit (register 14h, bit 0) = '1'. These are the Progressive Scan modes.

Table 16: Display Mode for Progressive Component TV (HDTV = '1')

Mode	IR[2:0]	VOS [1:0]	Input Data Format (Active Video)	Total Pixels/Line X Total Lines/Frame	Output Standard [TV Standard]	Frame Rate [Hz]	Pixel Clock [MHz]
61 [1]	000	11	720x480	858x525	ITU-R BT.1358 / EIA-770.1-A	30	13.500
62 [1]	001	11	720x576	864x625	ITU-R BT.1358	25	13.500

[1] These modes operate with interlaced input and progressive output.

Output Format Register

Symbol: **OF**
Address: **01h**
Bits: **2**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VOF1	VOF0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	0	0	1	1	1

VOF[1:0] (bits 7-6) of register OF control the video output format. Must be set per the table below:

Table 17: TV Output Configurations

VOF1	VOF0	TV Output Configuration
0	0	YCrCb
0	1	Composite, S-Video
1	0	YPrPb
1	1	SCART + Composite

Video Bandwidth Register

Symbol: **VBW**
Address: **02h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VBID	CFRB	CVBWB	CBW	YSV1	YSV0	YCV1	YCV0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	1	1	1	1	0

YCV[1:0] (bits 1-0) of register VBW control the filter used to limit the bandwidth of the luma signal in the CVBS output signal. A table of –3dB bandwidth values is given in Table 18 below.

YSV[1:0] (bits 3-2) of register VBW control the filter used to limit the bandwidth of the luma signal in the S-Video output signal. A table of –3dB bandwidth values is given in Table 18 below.

CBW (bit 4) of register VBW controls the filter used to limit the bandwidth of the chroma signal in the CVBS and S-Video output signals. A table of –3dB bandwidth values is given in Table 18 below.

Note that modes 61 & 66 are for HDTV application so the data for these modes does not go through the CBW, TSV or YCV bandwidth limiting filters.

Table 18: Video Bandwidth

Mode	CBW		YSV[1:0] and YCV[1:0]			
	0	1	00	01	10	11
37	0.709	0.979	2.630	3.070	4.050	6.720
38	0.466	0.643	1.730	2.020	2.660	4.410

CVBWB (bit 5) of register VBW controls the chroma component of the CVBS signal. CVBWB = '0' disables the chroma signal being added to the CVBS signal so the output on the CVBS pin is S-video luminance, CVBWB = '1' enables the chroma signal being added to the CVBS signal. Setting CVBWB = '0' enables the output of a black and white image on the composite output, thereby eliminating the degrading effects of the color signal (such as dot crawl and false colors). This is useful for viewing text with high accuracy. This also allows the output of either S-video or CVBS using just 2 DACs which is useful in situations where connector space is at a premium.

CFRB (bit 6) of register VBW controls whether the chroma sub-carrier free-runs, or is locked to the video signal. A '1' causes the sub-carrier to lock to the TV vertical rate, and should be used when the CIVEN bit (register 10h) is set to '0'. A '0' causes the sub-carrier to free-run, and should be used when the CIVEN bit is set to '1'.

VBID (bit 7) of register VBW controls the vertical blanking interval defeat function. A '1' in this register location forces the flicker filter to minimum filtering during the vertical blanking interval. A '0' in this location causes the flicker filter to remain at the same setting inside and outside of the vertical blanking interval.

Miscellaneous Register

Symbol: Misc
Address: 03h
Bits: 3

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	SAV8	HP8	VP8	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	1	0	1

SAV8, HP8 and VP8 (bits 5-3) of register Misc contain the MSB values for the start of active video, horizontal position and vertical position controls. They are described in detail in the SAV (address 04h), HP (address 05h) and VP (address 06h) register descriptions.

Start of Active Video Register

Symbol: SAV
Address: 04h
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SAV7	SAV6	SAV5	SAV4	SAV3	SAV2	SAV1	SAV0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	1	0	0	0	0

Register SAV controls the delay, in pixel increments, from leading edge of horizontal sync to start of active video. The entire bit field SAV[8:0] is comprised of this register SAV[7:0], plus SAV[8] contained in the Misc register (03h, bit 5). This is decoded as a whole number of pixels, which can be set anywhere between 0 and 511 pixels. Therefore, in any 2X clock mode the number of 2X clocks from the leading edge of Hsync to the first active data must be a multiple of two clocks.

Horizontal Position Register

Symbol: HP
Address: 05h
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	0	0	1	0	1

Register HP is used to shift the displayed TV image in a horizontal direction (left or right) to achieve a horizontally centered image on screen. The entire bit field, HP[8:0], is comprised of this register HP[7:0] plus HP[8] contained in the Misc register (03h, bit 4). Increasing values move the displayed image position right, and decreasing values move the image position left. Please note that these register bits cannot be all 0's.

Vertical Position Register

Symbol: VP
Address: 06h
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Register VP is used to shift the displayed TV image in a vertical direction (up or down) to achieve a vertically centered image on screen. The entire bit field, VP[8:0], is comprised of this register VP[7:0] plus VP[8] contained in the Misc register (03h, bit 3). The value represents the TV line number (relative to the VGA vertical sync) used to initiate the generation and insertion of the TV vertical interval (i.e. the first sequence of equalizing pulses). Increasing values delay the output of the TV vertical sync, causing the image position to move up on the TV screen. Decreasing values, therefore, move the image position DOWN. Each increment moves the image position by one TV line (approximately 2 input lines). The maximum value that should be programmed into VP[8:0] is the number of TV lines per field minus one half (262 or 312). When panning the image up, the number should be increased until (TVLPF-1/2) is reached, the next step should be to reset the register to zero. When panning the image down the screen, decrement the VP[8:0] value until the value zero is reached. The next step should set the register to TVLPF-1/2, and then decrement for further changes.

Black Level Register

Symbol: BL
Address: 07h
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	1	1

Register BL controls the black level. This allows control of the brightness independent of the pedestal level (see the description for register 4Fh). The luminance data is added to this black level, which must be set between 65 and 170. The default values for the black level are the same as the pedestal. When the input data format is 0 through 3 these values are 131 for NTSC and PAL-M with DACG[1:0] (register 21h) = '00', 109 for PAL with DACG[1:0] = '01' and 102 for NTSC-J with DACG[1:0] = '01'. When the input data format is 4 the default values are 112 for NTSC and PAL-M with DACG[1:0] = '10', 94 for PAL with DACG[1:0] = '11'and 88 for NTSC-J and SDTV YPrPb with DACG[1:0] = '11'. The default value is always 117 for HDTV YPrPb. The sugested BL setting for HDTV is between 117 and 170 with DACG[1:0] (Register 21h, bits 2-1) = '01' and BGBST (Register 14h, bit 7) = '1'. See also the description for the BLKEN bit (register 1Dh, bit 6).

Contrast Enhancement Register

Symbol: CE
Address: 08h
Bits: 3

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	CE2	CE1	CE0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	1	1

CE[2:0] (bits 2-0) of register CE control the contrast enhancement feature of the CH7206A, according to the figure below. A setting of '0' results in reduced contrast, a setting of '1' leaves the image contrast unchanged, and values beyond '1' result in increased contrast. [Note: The straight line denotes Yout = Yin and therefore no enhancement.]

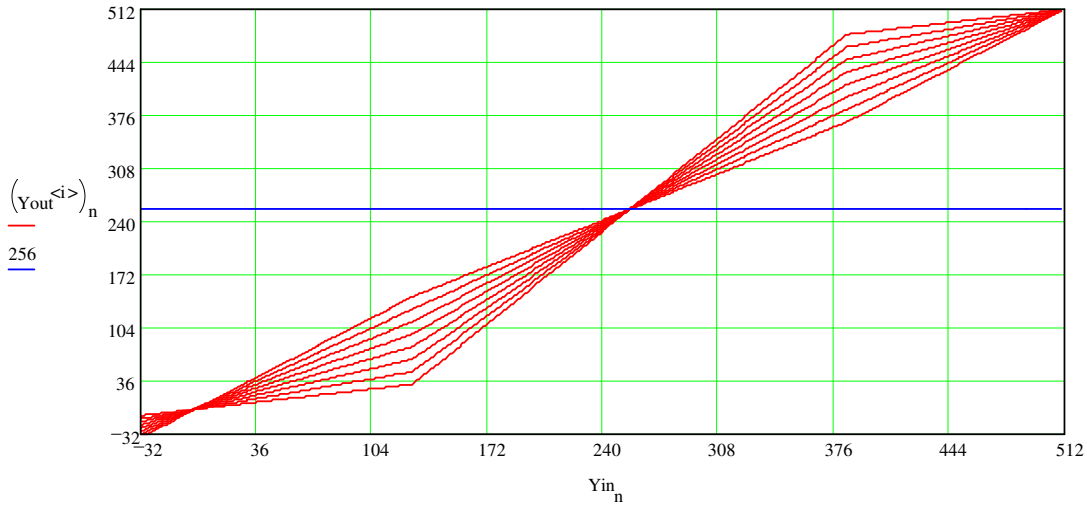

Figure 15: Contrast Enhancement of the CH7206A

TV PLL Control Register

Symbol: **TPC**
Address: **09h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	MEM2	MEM1	MEM0	N9	N8	M8	PLLCPI	PLLCAP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	1

PLLCAP (bit 0) of register TPC controls the TV PLL loop filter capacitor. A recommended listing of PLLCAP settings versus mode is given in the table below.

Table 19: PLLCAP setting vs. Display Mode

Mode	PLLCAP Value
37	1
38	1
48	1
60	1
61	1
62	1

PLLCPI (bit 1) of register TPC should be left at the default value.

M8 and N[9:8] (bits 4-2) of register TPC contain the MSB values for the TV PLL divider ratio's. These controls are described in detail in the PLLM (address 0Ah) and PLLN (address 0Bh) register descriptions.

MEM[0] (bit 5) of register TPC controls the input latch bias current level. The default value is recommended.

MEM[2:1] (bits 7-6) of register TPC control the memory sense amp reference level. The default value is recommended.

TV PLL M Value Register

Symbol: **PLLM**
Address: **0Ah**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	M7	M6	M5	M4	M3	M2	M1	M0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	0	0	0	0	1

Register PLLM controls the division factor applied to the 14.31818MHz frequency reference clock before it is input to the TV PLL phase detector when the CH7206A is operating in clock master mode. The entire bit field, M[8:0], is

comprised of this register M[7:0] plus M[8] contained in the TV PLL Control register (09h, bit2). In slave mode, an external pixel clock is used instead of the 14.31818MHz frequency reference, but the division factor is also controlled by M[8:0]. In slave mode, the value of 'M' is internally set to 1. A table of values versus display mode is given following the PLLN register description.

TV PLL N Value Register

Symbol: PLLN
Address: 0Bh
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N7	N6	N5	N4	N3	N2	N1	N0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	1	1	1

Register PLLN controls the division factor applied to the VCO output before being applied to the PLL phase detector, when the CH7206A is operating in clock master mode. The entire bit field, N[9:0], is comprised of this register N[7:0] plus N[9:8] contained in the TV PLL Control register (09h, bits 3 and 4). In slave mode, the value of 'N' is internally set to 1. The pixel clock generated in clock master modes is calculated according to the equation Fpixel = Fref * [(N+2) / (M+2)]. When using a 14.31818MHz frequency reference, the required M and N values for each mode are shown in the table below:

Table 20: TV PLL M and N values vs. Display Mode

Mode	Active Video Resolution, TV Standard	N 10-bits (dec)	N 10-bits (hex)	M 9-bits (dec)	M 9-bits (hex)
37	720x576, PAL, 1:1	31	0x1F	33	0x21
38	720x480, NTSC, 1:1	31	0x1F	33	0x21
61	720x480, ITU-R BT.1358 / EIA-770.1-A	33	0x21	31	0x1F
62	720x576, ITU-R BT.1358	33	0x21	31	0x1F

Sub-carrier Value Register

Symbol: FSCI
Address: 0Ch –0Fh
Bits: 8 each

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#	FSCI#
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:								

Registers FSCI contain a 32-bit value which is used as an increment value for the ROM address generation circuitry when CIVEN=0. The bit locations are specified as follows:

Register	Contents
0Ch	FSCI[31:24]
0Dh	FSCI[23:16]
0Eh	FSCI[15:8]
0Fh	FSCI[7:0]

When the CH7206A is used in the clock master mode, the tables below should be used to set the FSCI registers. When using these values, the CIVEN bit in register 10h should be set to '0', and the CFRB bit in register 02h should be set to '1'.

Table 21: FSCI Values (525-Line TV-Out Modes)

Mode	NTSC "Normal Dot Crawl" (dec)	NTSC "Normal Dot Crawl" (hex)	PAL-M "Normal Dot Crawl" (dec)	PAL-M "Normal Dot Crawl" (hex)
38	569,408,543	0x21F07C1F	568,782,819	0x21E6EFE3

Table 22: FSCI Values (625-Line TV-Out Modes)

Mode	PAL "Normal Dot Crawl"	PAL-N "Normal Dot Crawl"
37	705,268,427	569,807,942

CIV Control Register

Symbol: CIVC
Address: 10h
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SICP	SICN	CIV25	CIV24	CIVC1	CIVC0	PALN	CIVEN
TYPE:	R/W	R/W	R	R	R	R	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	1

CIVEN (bit 0) of register CIVC controls whether the FSCI value is used to set the sub-carrier frequency, or the automatically calculated (CIV) value. When the CIVEN value is '1', the number calculated and present at the CIV registers will automatically be used as the increment value for sub-carrier generation. Whenever this bit is set to '1', the CFRB bit should be set to '0'.

PALN (bit 1) of register CIVC forces the CIV algorithm to generate the PAL-N (Argentina) sub-carrier frequency when it is set to '1'. When this bit is set to '0', the VOS[1:0] value is used by the CIV algorithm to determine which sub-carrier frequency to generate.

CIVC[1:0] (bits 3-2) of register CIVC control the hysteresis circuit which is used to calculate the CIV value. The default value should be used.

CIV[25:24] (bits 5-4) of register CIVC contain the MSB values for the calculated increment value (CIV) readout. This is described in detail in the CIV (address 11h-13h) register description.

SICP and SICN (bits 7-6) of register CIVC enable the Serial Port. The default value is recommended.

Calculated Increment Value Register

Symbol: **CIV**
Address: **11h –13h**
Bits: **8 each**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CIV#	CIV#	CIV#	CIV#	CIV#	CIV#	CIV#	CIV#
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

Registers CIV contain the value that was calculated by the CH7206A as the sub-carrier increment value. The entire bit field, CIV[25:0], is comprised of these three registers CIV[23:0] plus CIV[25:24] contained in the CIV Control register (10h, bits 4 and 5). This value is used when the CIVEN bit is set to '1'. The bit locations are specified below.

Register	Contents
10h	CIV[25:24]
11h	CIV[23:16]
12h	CIV[15:8]
13h	CIV[7:0]

HDTV Mode Register

Symbol: **HDTVM**
Address: **14h**
Bits: **2**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BGBST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HDTV
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	0

HDTV (bit 0) of register HDTVM toggles between SDTV and HDTV modes.
HDTV = 0 => enables SDTV modes 37, 38
= 1 => enables YPrPb modes 48, 60, 61, 62

BGBST (bit 7) of register CB boost the bandgap voltage which controls the DAC output by 6% when set to 1. This has the effect of boosting the DAC output by about 6%. The recommended value is 1.

Clock Mode Register

Symbol: **CM**
Address: **1Ch**
Bits: **4**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	M/S*	MCP	PCM	XCM
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	1	1

XCM (bit 0) of register CM signifies the XCLK frequency for the data input. A value of '0' is used when XCLK is at the pixel frequency (dual edge clocking mode) and a value of '1' is used when XCLK is twice the pixel frequency (single edge clocking mode).

PCM (bit 1) of register CM controls the P-Out clock frequency. A value of '0' generates a clock output at the pixel frequency, while a value of '1' generates a clock at twice the pixel frequency.

MCP (bit 2) of register CM controls the phase of the XCLK clock input for the data input. A value of '1' inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching input data.

M/S* (bit 3) of register CM controls whether the device operates in master or slave clock mode. In master mode (M/S* = '1'), the 14.31818MHz clock is used as a frequency reference in the TV PLL, and the M and N values are used to determine the TV PLL's operating frequency. In slave mode (M/S* = '0') the XCLK input is used as a reference to the TV PLL. The M and N TV PLL divider values are forced to one.

Input Clock Register

Symbol: IC
Address: 1Dh
Bits: 5

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	BLKEN	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	1	0	0	0

XCMD[3:0] (bits 3-0) of register IC control the delay applied to the XCLK signal before latching input data D[11:0] per the following table. 1 unit is approximately 70 ps worst case.

Table 23: Delay applied to XCLK before latching input data D[11:0]

XCMD3	XCMD2	XCMD1	XCMD0	Adjust phase of Clock relative to Data
0	0	0	0	0 * t_{STEP}, XCLK ahead of Data
0	0	0	1	1 * t_{STEP}, XCLK ahead of Data
0	0	1	0	2 * t_{STEP}, XCLK ahead of Data
0	0	1	1	3 * t_{STEP}, XCLK ahead of Data
0	1	0	0	4 * t_{STEP}, XCLK ahead of Data
0	1	0	1	5 * t_{STEP}, XCLK ahead of Data
0	1	1	0	6 * t_{STEP}, XCLK ahead of Data
0	1	1	1	7 * t_{STEP}, XCLK ahead of Data
1	0	0	0	0 * t_{STEP}, XCLK behind Data
1	0	0	1	1 * t_{STEP}, XCLK behind Data
1	0	1	0	2 * t_{STEP}, XCLK behind Data
1	0	1	1	3 * t_{STEP}, XCLK behind Data
1	1	0	0	4 * t_{STEP}, XCLK behind Data
1	1	0	1	5 * t_{STEP}, XCLK behind Data
1	1	1	0	6 * t_{STEP}, XCLK behind Data
1	1	1	1	7 * t_{STEP}, XCLK behind Data

BLKEN (bit 6) of register IC controls the Black Level control register update during the vertical sync blanking period. A value of '0' disables the Black Level control register update. A value of '1' enables the Black Level control register update.

GPIO Control Register

Symbol: GPIO
Address: 1Eh
Bits: 6

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	GOENB1	GOENB0	GPIOL1	GPIOL0	Reserved	Reserved	POUTE	POUTP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	1	0	0	1	0

POUTP (bit 0) of register GPIO controls the polarity of the P-Out signal. A value of '0' does not invert the clock at the output pad.

POUTE (bit 1) of register GPIO enables the P-Out signal. A value of '1' drives the P-Out clock signal out of the P-Out pin. A value of '0' disables the P-Out signal.

GPIOL[1:0] (bits 5-4) of register GPIO define the GPIO Read or Write Data bits [1:0]. When the corresponding GOENB bits (GOENB[1:0], are '0', the values in GPIOL[1:0] are driven out at the corresponding GPIO pins. When the corresponding GOENB bits are '1', the values in GPIOL[1:0] can be read to determine the level forced into the corresponding GPIO pins. Note that the default state of GPIOLx depends on the state of the GPIOx pins since by default these pins are configured as inputs. With no external pullup or pulldown the internal pullup causes GPIOLx to be '1'.

GOENB[1:0] (bits 7-6) of register GPIO define the GPIO Direction Control bits [1:0]. GOENB[1:0] control the direction of the GPIO[1:0] pins. A value of '1' sets the corresponding GPIO pin to an input, and a value of '0' sets the corresponding pin to a non-inverting output. The level at the output depends on the value of the corresponding bit GPIOL[1:0].

Input Data Format Register

Symbol: IDF
Address: 1Fh
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	IBS	DES	SYO	VSP	HSP	IDF2	IDF1	IDF0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	0	0	1	0	0

IDF[2:0] (bits 2-0) of register IDF select the input data format for the D[11:0] input. See section 2.3.4 for a listing of available formats.

HSP (bit 3) of register IDF controls the horizontal sync polarity. A value of '0' defines the horizontal sync to be active low, and a value of '1' defines the horizontal sync to be active high.

VSP (bit 4) of register IDF controls the vertical sync polarity. A value of '0' defines the vertical sync to be active low, and a value of '1' defines the vertical sync to be active high.

SYO (bit 5) of register IDF controls the sync direction. A value of '0' defines sync to be input to the CH7206A, and a value of '1' defines sync to be output from the CH7206A.

DES (bit 6) of register IDF signifies when the CH7206A is to decode embedded sync signals present in the input data stream instead of using the H and V pins. This feature is only available for input data format # 4. A value of '0' selects the H and V pins to be used as the sync inputs, and a value of '1' selects the embedded sync signal.

IBS (bit 7) of register IDF selects the data and clock input buffer type for the data input D[11:0] according to the following table:

Table 24: D1 Input Buffer Type Selection

IBS	Data Input Buffer Type
0	CMOS, single ended type for clock and data
1	Differential (clock) and comparator (data) type

Connection Detect Register

Symbol: CD
Address: 20h
Bits: 6

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	XOSC2	Reserved	DACT3	DACT2	DACT1	DACT0	SENSE
TYPE:	R/W	R/W	R/W	R	R	R	R	R/W
DEFAULT:	0	1	0	X	X	X	X	0

DACT[3:0] (bits 4-1) and SENSE (bit 0) of register CD provide a means to sense the connection of a TV to the four DAC outputs. The status bits, DACT[3:0] correspond to the termination of the four DAC outputs. However, the values contained in these status bits ARE NOT VALID until a sensing procedure is performed. Use of this register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits. The detection sequence works as follows:

1) Set the power management register (address 49h) to enable all DACs.
2) Set the SENSE bit to a 1. This forces a constant output from the DACs. Note that during SENSE = 1, these 4 analog outputs are at steady state and no TV synchronization pulses are asserted.
3) Reset the SENSE bit to 0. This triggers a comparison between the voltage present on these analog outputs and the reference value. During this step, each of the four status bits corresponding to individual DAC outputs will be reset to "0" if they are NOT CONNECTED.
4) Read the status bits. The status bits, DACT[3:0] now contain valid information which can be read to determine which outputs are connected to a TV. Again, a "1" indicates a valid connection, a "0" indicates an unconnected output.

XOSC2 (bit 6) of register CD contains the MSB value for the XOSC (crystal oscillator gain control) word. The entire bit field, XOSC[2:0], is comprised of this bit plus XOSC[1:0] contained in the DAC Control register (address 21h, bits 7-6).

DAC Control Register

Symbol: **DC**
Address: **21h**
Bits: **7**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	XOSC1	XOSC0	Reserved	SYNCO1	SYNCO0	DACG1	DACG0	DACBP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

DACBP (bit 0) of register DC selects the DAC bypass mode. A value of '1' outputs the incoming data directly at the DAC[3:0] outputs for the VGA-Bypass RGB output. For the other TV output modes such as S-Video, RCA, SCART and YPrPb, DACBP bit must be set to 0.

DACG[1:0] (bits 2-1) of register DC control the DAC gain. DACG0 should be set to '0' for NTSC and PAL-M video standards, and '1' for PAL and NTSC-J video standards. DACG1 should be '0' when the input data format is RGB (IDF = 0-3), and '1' when the input data format is YCrCb (IDF = 4). If the output format is HDTV YPrPb, DACG[1:0] should be set as 01, regardless of the input data format.

SYNCO[1:0] (bits 4-3) of register DC select the signal to be output from the GPIO1/CHSync pin according to in Table 25 below.

Table 25: Composite / Horizontal Sync Output

SYNCO[1:0]	Composite / Horizontal Sync Output
00	No Output
01	Reserved
10	TV Composite Sync
11	TV Horizontal Sync

XOSC[1:0] (bits 7-6) of register DC control the crystal oscillator. The entire bit field, XOSC[2:0], is comprised of XOSC[1:0] from this register plus XOSC2 contained in the Connection Detect register (20h, bit 6).The default value is recommended.

Buffered Clock Output Register

Symbol: **BCO**
Address: **22h**
Bits: **5**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	BCOEN	BCOP	BCO2	BCO1	BCO0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	1

BCO[2:0] (bits 2-0) of register BCO select the signal output at the BCO pin, according to the table below:

Table 26: BCO Output Signal

BCO[2:0]	Buffered Clock Output	BCO[2:0]	Buffered Clock Output
000	The 14MHz crystal	100	Sine ROM MSB
001	The 27MHz crystal	101	Cosine ROM MSB
010	Reserved	110	VGA Vertical Sync
011	Field ID	111	TV Vertical Sync

BCOP (bit 3) of register BCO selects the polarity of the BCO output. A value of '1' does not invert the signal at the output pad.

BCOEN (bit 4) of register BCO enables the BCO output pin. When BCOEN is high, the BCO pin will output the selected signal. When BCOEN is low, the BCO pin will be held in tri-state mode.

Reset Register

Symbol: RST
Address: 48h
Bits: 5

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	GPHSS	Reserved	Reserved	ResetIB	ResetDB	Reserved	TSTP1	TSTP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	0	0	0

TSTP[1:0] (bits 1:0) of register STP enable and select test pattern generation (color bar, ramp). The pattern generated is determined by the table below:

Table 27: Test Pattern Selection

TSTP1	TSTP0	Test Pattern
0	0	No test pattern – Input data is used
0	1	Color Bars
1	0	Horizontal Luminance Ramp
1	1	Horizontal Luminance Ramp

ResetDB (bit 3) of register STP resets the datapath. When ResetDB is '0' the datapath is reset. When ResetDB is '1' the datapath is enabled. The datapath is also reset at power on by an internally generated power-on-reset signal.

ResetIB (bit 4) of register STP resets all control registers (addresses 00h – 7Fh). When ResetIB is '0' the control registers are reset to the default values. When ResetIB is '1' the control registers operate normally. The control registers are also reset at power on by an internally generated power on reset signal.

GPHSS (bit 7) of register CD controls the selection of the signal on the GPIO1 pin when configured as an output.

GPHSS = 0 => Signal on GPIO1 is GPIOL1 (register 1Eh, bit 5) when GOENB1 = '0' (register 1Eh , bit 7)
= 1 => Signal on GPIO1 is HSYNC when GOENB1 = '0' (register 1Eh , bit 7)

Power Management Register

Symbol: PM
Address: 49h
Bits: 5

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	DACPD3	DACPD2	DACPD1	DACPD0	TVPD
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

TVPD (bit 0) of register PM controls power down. When TVPD is '0' the CH7206A is ON. When TVPD is '1' the CH7206A is in power down mode.

DACPD[3:0] (bits 4:1) of register PM control DAC0 through DAC3 Power Down. DAC0 through DAC3 will be turned on only if TVPD bit is set to '0'. If TVPD bit is set to '1', then DAC0 through DAC3 will be in power down state regardless of DACPD0 through DACPD3 state.

Table 28: DAC Power Down Control

TVPD	DACPD[3:0]	Operating State	Functional Description
0	0000	Normal (On)	All DACs on
0	0001		DAC 0 powered down, DACs 1, 2, 3on
0	0010		DAC 1 powered down, DACs 0, 2, 3 on
0	0100		DAC 2 powered down, DACs 0, 1, 3 on
0	1000		DAC 3 powered down, DACs 0, 1, 2 on
1	xxxx	Full Power Down	All circuitry is powered down except serial port

Version ID Register

Symbol: VID
Address: 4Ah
Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	1	0	0	0	0	0	0	0

Register VID is a read only register containing the version ID number of the CH7206A.

CH7206A VID is 80h

Device ID Register

Symbol: **DID**
Address: **4Bh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	1	1	1	1	1

Register DID is a read only register containing the device ID number of the CH7206A family.

CH7206A DID is 1Fh

Pedestal Level Control Register

Symbol: **PEDL**
Address: **4Fh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	PEDL7	PEDL6	PEDL5	PEDL4	PEDL3	PEDL2	PEDL1	PEDL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	1	1

Register PEDL defines the pedestal level. This allows control of the pedestal level independent of the black level. When the input data format is 0 through 3 the correct values are 131 for NTSC and PAL-M, 109 for PAL and 102 for NTSC-J. When the input data format is 4 the correct values are 112 for NTSC and PAL-M, 94 for PAL and 88 for NTSC-J and YPrPb.

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All power supplies relative to GND	-0.5		5.0	V
	Input voltage of all digital pins	GND – 0.5		VDD + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	0		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (1 minute)			220	°C

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latchup.

4.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	PLL Power Supply Voltage	3.1	3.3	3.6	V
VDD	DAC Power Supply Voltage	3.1	3.3	3.6	V
DVDD	Digital Power Supply Voltage	3.1	3.3	3.6	V
VDDV	I/O Power Supply Voltage	1.1	1.8	3.6	V
R_L	Output load to DAC Outputs		37.5		Ω

4.3 Electrical Characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD =3.3V ± 5%)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		33.9		mA
	Video level error			10	%
I_{VDD}	Total supply current		200		mA
I_{VDDV}	VDDV (1.8V) current (15pF load on P-out)		4		mA
I_{PD}	Total Power Down Current		0.06		mA

4.4 Digital Inputs / Outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Inputs		0.25			V
V_{DATAIH}	D[0-11] Input High Voltage		Vref+0.25		DVDD+0.5	V
V_{DATAIL}	D[0-11] Input Low Voltage		GND-0.5		Vref-0.25	V
V_{MISCIH}	GPIOx, RESET* Input High Voltage	DVDD=3.3V	2.7		VDD + 0.5	V
V_{MISCIL}	GPIOx, RESET* Input Low Voltage	DVDD=3.3V	GND-0.5		0.6	V
I_{MISCPU}	Pull Up Current (GPIO, RESET*)	V_{IN} = 0V	0.5		5.0	uA
V_{MISCOH}	GPIOx, BCO, H, V Output High Voltage	I_{OH} = -0.4mA	DVDD-0.2			V
V_{MISCOL}	GPIOx, BCO, H, V Output Low Voltage	I_{OL} = 3.2mA			0.2	V
$V_{P-OUTOH}$	P-OUT Output High Voltage	I_{OH} = - 0.4mA	VDDV-0.2			V
$V_{P-OUTOL}$	P-OUT Output Low Voltage	I_{OL} = 3.2 mA			0.2	V

Note :

V_{DATA} - refers to all digital data (D[11:0]), clock (XCLK, XCLK*) and sync (H, V) inputs. V_{MISC} - refers to GPIOx, and RESET* inputs and GPIOx,, BCO/VSYNC outputs and H, V when configured as outputs (SYO=1).

4.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{XJIT}	XCLK clock jitter tolerance			2		ns
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	XCLK = XCLK* to D[11:0], H, V, DE = Vref	0.35			ns
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	D[11:0], H, V, DE = Vref to XCLK = XCLK*	0.5			ns
t_R	Pout, H and V (when configured as outputs) Output Rise Time (20% - 80%)	15pF load DVDD, VDDV = 3.3V			1.50	ns
t_F	Pout, H and V (when configured as outputs) Output Fall Time (20% - 80%)	15pF load DVDD, VDDV = 3.3V			1.50	ns
t_{STEP}	De-skew time increment		50		80	ps

4.6 Timing Information

4.6.1 Clock - Slave, Sync - Slave Mode

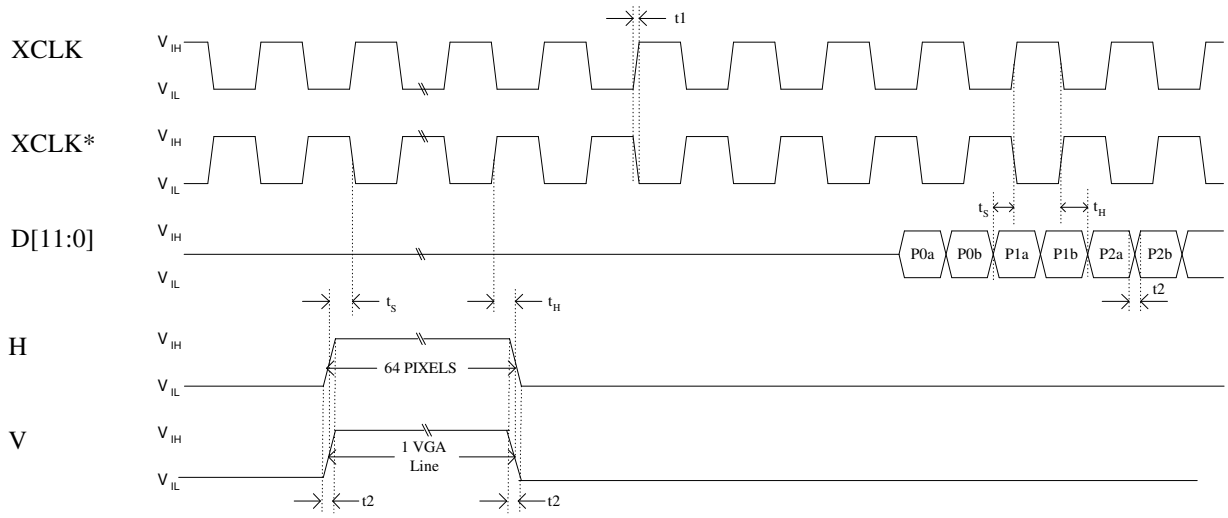

Figure 16: Timing for Clock - Slave, Sync - Slave Mode

Table 29: Timing for Clock - Slave, Sync - Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_H	Hold Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0], H, V rise/fall time w/ 15pF load		1		ns

4.6.2 Clock - Master, Sync - Slave Mode

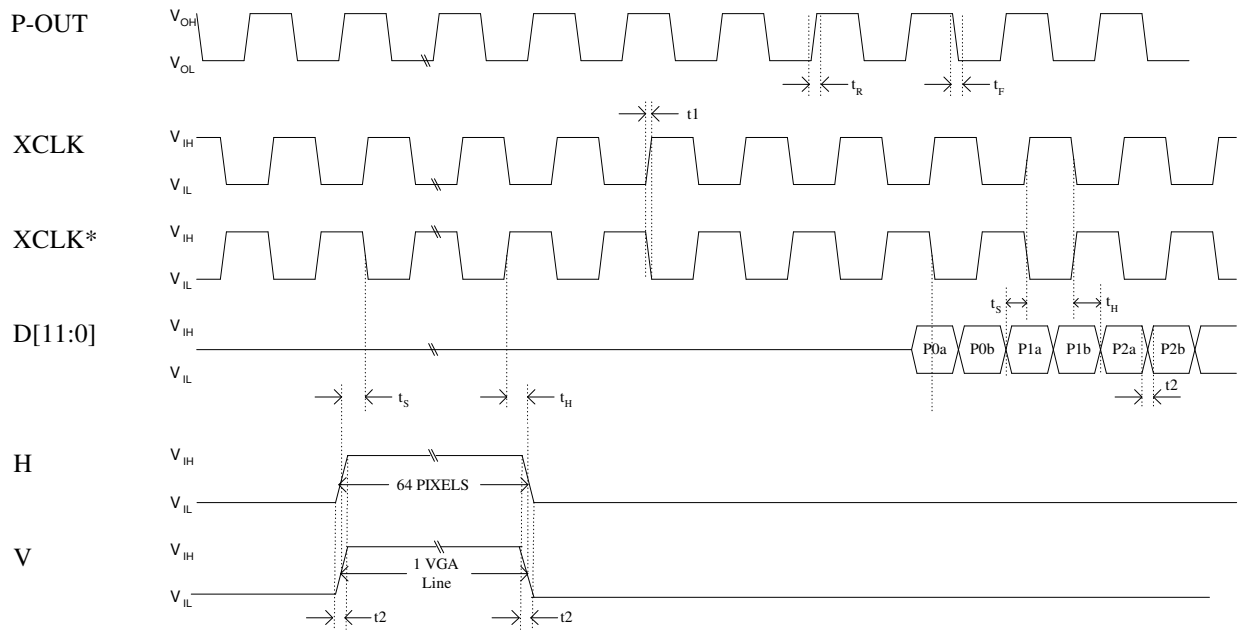

Figure 17: Timing for Clock - Master, Sync - Slave Mode

Table 30: Timing for Clock - Master, Sync - Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_H	Hold Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_R	Pout Output Rise Time	see section 4.5			
t_F	Pout Output Fall Time	see section 4.5			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0], H, V rise/fall time w/15pF load		1		ns

4.6.3 Clock - Master, Sync - Master Mode

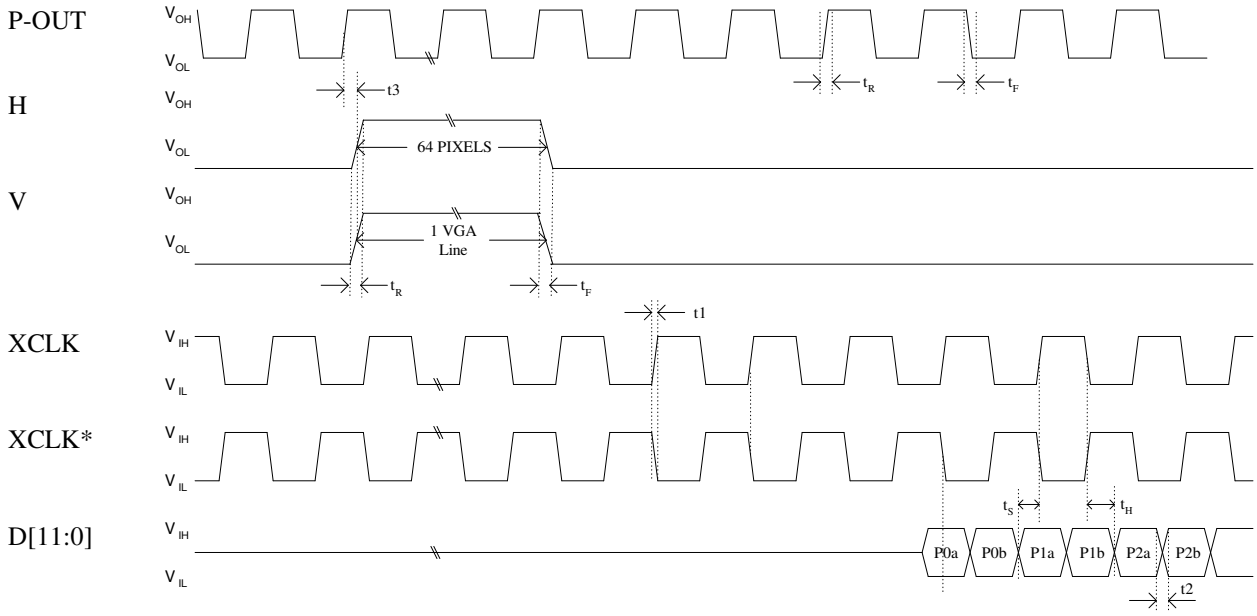

Figure 18: Clock - Master, Sync - Master Mode

Table 31: Timing for Clock - Master, Sync - Master Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_H	Hold Time: D[11:0], H, V to XCLK, XCLK*	see section 4.5			
t_R	Pout, H, V (when configured as outputs) Output Rise Time	see section 4.5			
t_F	Pout, H, V (when configured as outputs) Output Fall Time	see section 4.5			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0] rise/fall time w/15pF load		1		ns
t3	Hold time: P-OUT to HSYNC, VSYNC delay		1.5		ns

5.0 PACKAGE DIMENSIONS

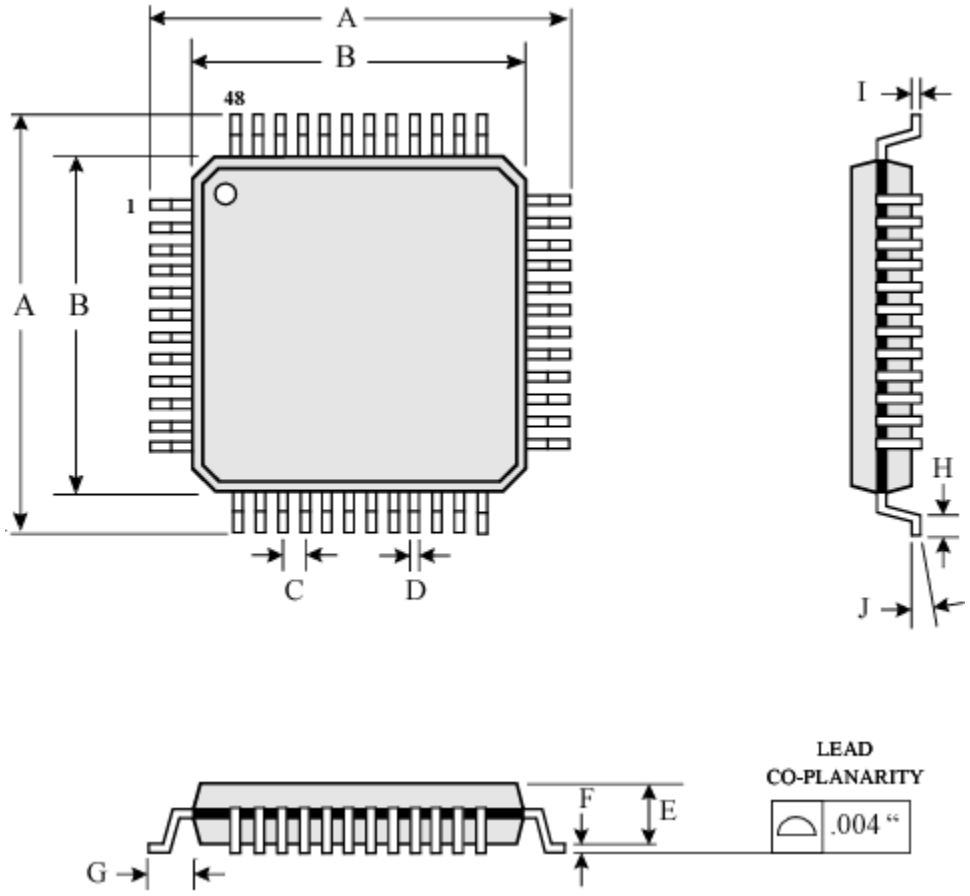

Figure 19: 48 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
48 (7 X 7 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	9	7	0.5	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

6.0 REVISION HISTORY

Table 32: Revisions

Revision #	Date	Section	Description
1.0	4/24/2003	All	1st Official Release
1.1	6/13/03	3.3, register 07h	Updated black level register description
		3.3, register 1Eh	Updated GPIO register description
		4.3	Updated Electrical Characteristics
	10/03/03	Table 16	Removed modes 48 and 60
		Table 18	Removed modes 48, 60, 61, and 62
		Table 20	Removed modes 48 and 60
1.2	4/09/2013	Ordering Information	Changed CH7206A-D to CH7206A-DF. Added CH7206A-DF-TR.

Disclaimer

This document provides technical information for the user. Chrontel reserves the right to make changes at any time without notice to improve and supply the best possible product and is not responsible and does not assume any liability for misapplication or use outside the limits specified in this document. We provide no warranty for the use of our products and assume no liability for errors contained in this document. The customer should make sure that they have the most recent data sheet version. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Chrontel, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Chrontel PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF Chrontel. Life support systems are those intended to support or sustain life and whose failure to perform when used as directed can reasonably expect to result in personal injury or death.

ORDERING INFORMATION			
Part Number	Package Type	Number of Pins	Voltage Supply
CH7206A-DF	LQFP, Lead Free	48	3.3V
CH7206A-DF-TR	LQFP, Lead Free, Tape & Reel	48	3.3V

Chrontel

2210 O'Toole Avenue, Suite 100,
San Jose, CA 95131-1326
Tel: (408) 383-9328
Fax: (408) 383-9338
www.chrontel.com
E-mail: sales@chrontel.com

©2013 Chrontel, Inc. All Rights Reserved.
Printed in the U.S.A.