
CH7212A DisplayPort to VGA Converter on USB Type C

FEATURES

- Compliant with DisplayPort Alternate Mode on USB Type C standard
- Compliant with DisplayPort Specification version 1.3 and Embedded DisplayPort (eDP) Specification version 1.4
- Support two link lane at 1.62Gbps, 2.7Gbps (HBR) or 5.4Gbps (HBR2) link rate
- Automotive DP input signal detection
- DP_BR signaling modes supported
- DP Lane Swap supported for Type-C Receptacle
- DisplayPort receiver auto equalization supported for the compensation of input signal attenuation
- Support Analog RGB output for VGA with Triple 9-bit DAC up to 240MHz pixel rate. Sync signals can be provided in separated or composite manner. Support VESA and CEA timing standards up to 2048x1536@60Hz with reduced blanking
- VGA output is compliant with VESA VSIS v1r2 specification
- DAC connection detection supported
- 2 CC Ports support Charge-Through
- USB Power Delivery control module supported with HPD to PD converter integrated
- Support CDP and DCP mode of Battery Charging Specification Revision 1.2
- Active DDC buffer and related control register integrated
- IIC-over-AUX transaction supported
- AUX Switch integrated for USB Plug Orientation Switch
- Embedded MCU to handle the control logic
- USB billboard module integrated
- USB 2.0 PHY supported with internal switch for data/file transport in USB full speed mode
- Fast Role Swap supported
- On-chip Audio encoder which support 2 channel IIS/S/PDIF audio output
- Support device boot up by loading firmware from the embedded EEPROM automatically, integrated EDID Buffer
- MCCS bypass supported
- IIC slave and USB 2.0 interface are available for firmware update and debug
- Crystal free supported
- Support Auto Power Saving mode and low stand-by current
- Anti-back drive support
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 48-Pin QFN package (6 x 6 mm)

GENERAL DESCRIPTION

Chrontel's CH7212A is a low-cost, low-power semiconductor device that translates the DisplayPort signal to VGA through the USB Type-C connector. This innovative USB Type-C based DisplayPort receiver with an integrated VGA Encoder is specially designed to target the USB Type-C to VGA converter, adopter and docking device. Through the CH7212A's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized multimedia data can be seamlessly converted to VGA output.

The CH7212A is compliant with the DisplayPort specification version 1.3 and the Embedded DisplayPort Specification version 1.4. In the device's receiver block, which supports two DisplayPort Main Link Lanes input with data rate running at 1.62Gb/s, 2.7Gb/s or 5.4Gb/s, can accept RGB digital formats in either 18-bit 6:6:6 or 24-bit 8:8:8, and converted the input signal to VGA output up to 2048x1536@60Hz with reduced blanking. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7212A is capable of instantly bring up the video display to the VGA monitor when the initialization process is completed between CH7212A and the graphic chip.

The DACs are based on current source architecture. And the VGA output meet VESA VSIS v1r2 clock jitter target. With sophisticated MCU and the embedded EEPROM, CH7212A support auto-boot and EDID buffer. After the configuration by firmware, which is auto loaded from the EEPROM embedded, CH7212A supports DisplayPort input detection, DAC connection detection and determine to enter into power saving mode automatically.

APPLICATION

- USB Type C to VGA cable/Adapter/Docking Station

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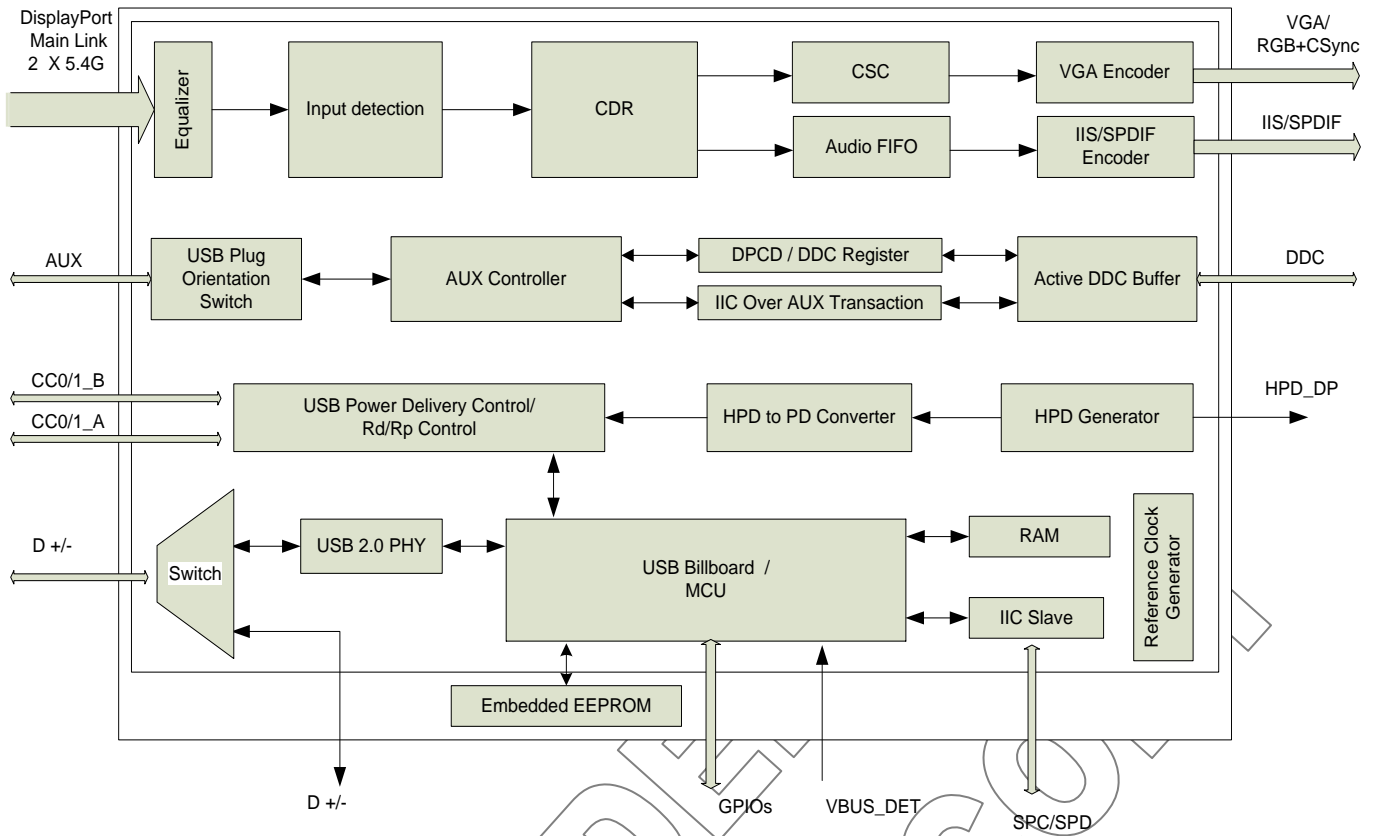


Figure 1: CH7212A Functional Block Diagram

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1.0 PIN-OUT

1.1 Package Diagram

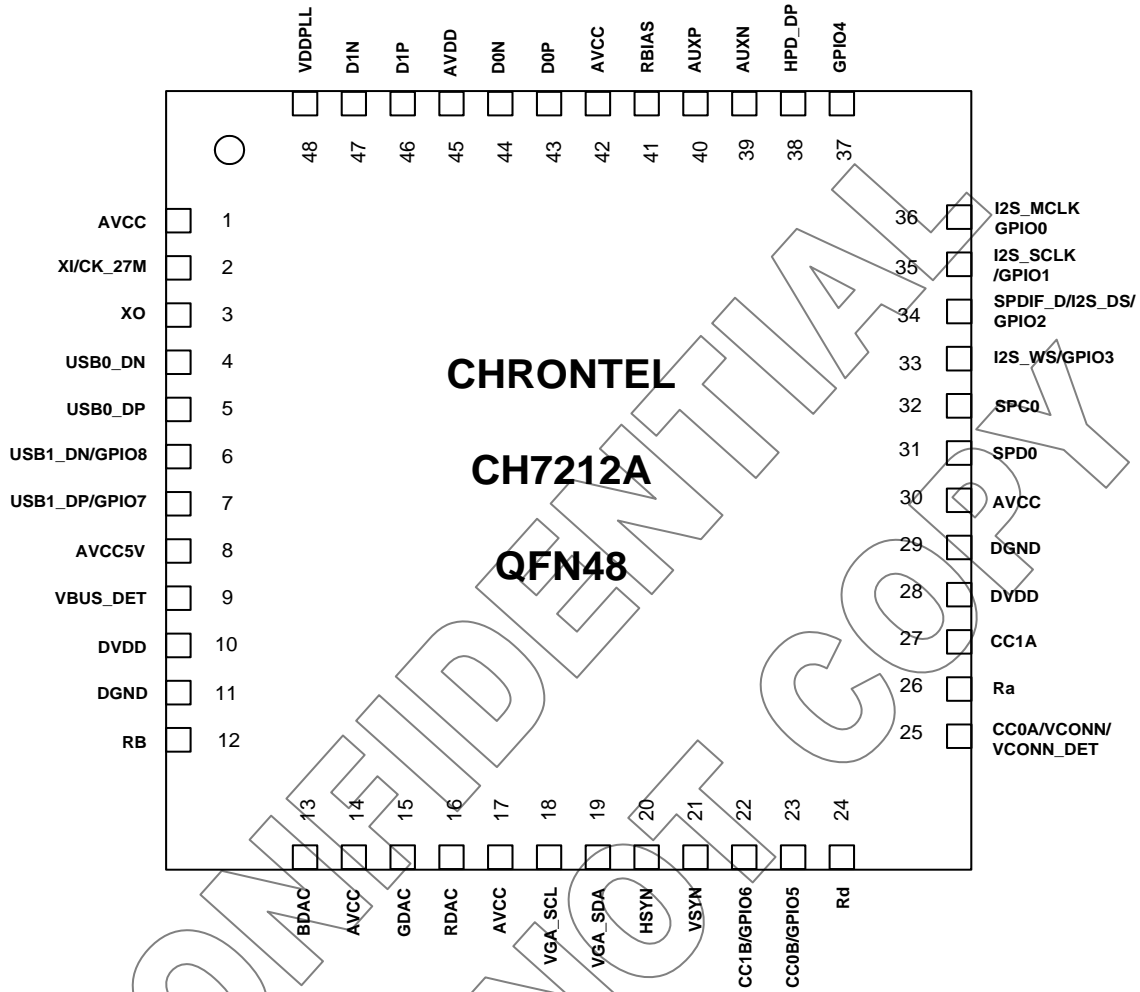


Figure 2: CH7212A 48-Pin QFN Pin Out

1.2 Pin Description

Table 1: 48 QFN Pin Name Descriptions

Pin #	Type	Symbol	Description
2	In	XI	Crystal Input / External Reference Input A parallel resonance crystal should be attached between this pin and XO. An external 3.3V CMOS compatible clock also can drive the XI Input. This pin can be reserved and left open in normal application.
3	Out	XO	Crystal Output A parallel resonance crystal should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open. This pin can be reserved and left open in normal application.
4,5	In/Out	USB0_DN/ USB0_DP	D+/- Input of USB Type C Interface
6	In/Out	USB1_DN	USB 2.0 Output Pins
	In/Out	GPIO8	General Purpose Input/Output
7	In/Out	USB1_DP	USB 2.0 Output Pins
	In/Out	GPIO7	General Purpose Input/Output
9	In	VBUS_DET	USB VBUS Voltage Detection Voltage input 0 ~ 5V
12	In	RB	Reset* Input (Internal pull-up) When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
13	Out	BDAC	VGA Blue Component Output
15	Out	GDAC	VGA Green Component Output
16	Out	RDAC	VGA Red Component Output
18	Out	VGA_SCL	Serial Port Clock Output to VGA Receiver The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 k _Ω resistor to the desired voltage level
19	In/Out	VGA_SDA	Serial Port Data to VGA Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 k _Ω resistor to the desired voltage level
20	Out	HSYN	Horizontal Sync Signal Output The amplitude of this pin is from 0 to AVCC
21	Out	VSYN	Vertical Sync Signal Output The amplitude of this pin is from 0 to AVCC
22	In/Out	CC1B	Downstream Type-C Port Configuration Channel 2
	In/Out	GPIO6	General Purpose Input/Output
23	In/Out	CC0B	Downstream Type-C Port Configuration Channel 1
	In/Out	GPIO5	General Purpose Input/Output
24	In	Rd	Upstream Type-C Port CC1A Rd Connection
25	In/Out	CC0A	Upstream Type-C Port Configuration Channel 1
	In	VCONN	VCONN Power Supply (2.7V~5V)
	In/Out	VCONN_DET	Scaled Input for VCONN Voltage Level Detection
31	In/Out	SPD0	Slave Serial Port Data Input / Output This pin functions as the data pin of the serial port. External pull-up 6.8 k _Ω Resistor is required.

32	In	SPC0	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up 6.8 K Ω resistor is required
33	Out	I2S_WS	WS of I2S audio output
	In/Out	GPIO3	General Purpose Input/Output
34	Out	SPDIF_D	SPDIF audio output
	Out	I2S_SD	SD of I2S audio output
	In/Out	GPIO2	General Purpose Input/Output
35	Out	I2S_SCLK	SCLK of I2S audio output
	In/Out	GPIO1	General Purpose Input/Output
36	Out	I2S_MCLK	MCLK of I2S audio output
	In/Out	GPIO0	General Purpose Input/Output
37	In/Out	GPIO4	General Purpose Input/Output
38	Out	HPD_DP	Hot-Plug signal for Display Port
39,40	In/Out	AUXN/AUXP	AUX Channel Differential Input/Output These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
41	In	RBIAS	Analog Reference Control Resistor A 1K-ohm with 1% tolerance resistor should be connected between this pin and ground using short and wide traces.
43,44	In	D0P/ D0N	DP Main Link Differential Lane 0 Input These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
46/47	In	D1P/ D1N	DP Main Link Differential Lane 1 Input These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
1,14,17,30,42	Power	AVCC	Analog Power Supply (3.3V)
8	Power	AVCC5V	Analog Power Supply (5V)
10,28	Power	DVDD	Digital Core/IO Power Supply (1.2V)
11,29	Power	DGND	Digital Ground
17	Power	AVDDPLL	PLL Power Supply (1.2V)
45	Power	AVDD	Analog Power Supply (1.2V)
48	Power	VDDPLL	PLL Power Supply (1.2V)

2.0 PACKAGE DIMENSION

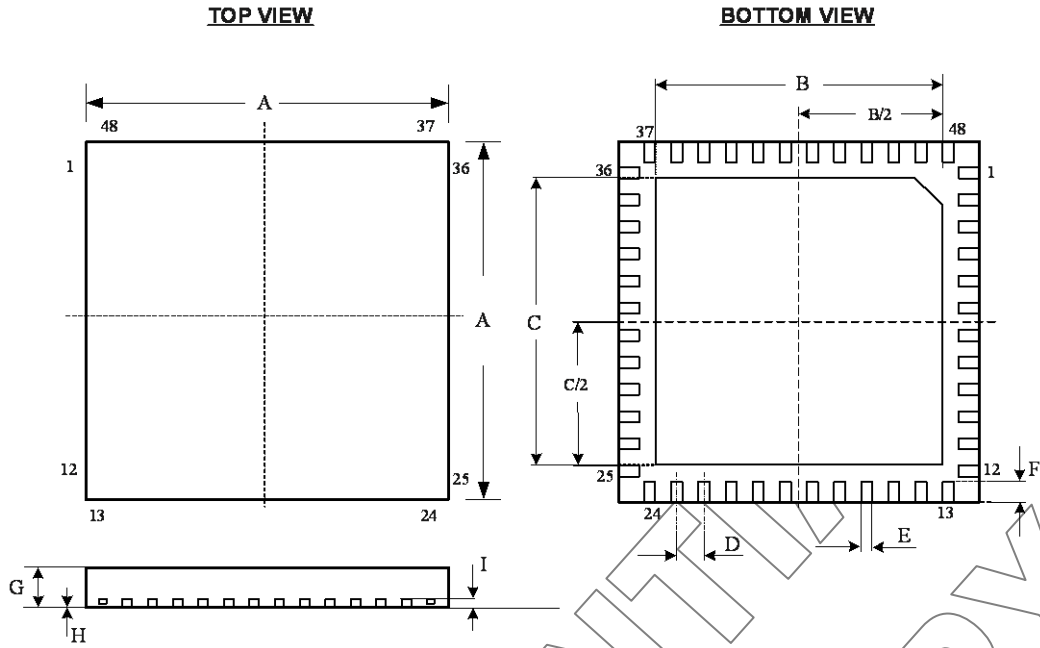


Figure 3: 48 Pin QFN Package

Table of Dimensions

No. of Leads		SYMBOL								
48 (6 X 6 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	5.90	4.35	4.35	0.4	0.13	0.30	0.7	0	0.20
	MAX	6.10	4.65	4.65		0.25	0.50	0.8	0.05	0.203

Notes:

Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION			
Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7212A-BF	48 QFN, Lead-free	Commercial: 0 to 70°C	490/Tray

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