PCB Layout and Design Guide for CH7219

1.0 INTRODUCTION

Chrontel's CH7219 is specially designed to target the USB Type-C to HDMI converter, adapter and docking device. The CH7219's DP/eDP receiver is compliant with the DisplayPort Specification 1.4 and Embedded DisplayPort (eDP) Specification version 1.4. With sophisticated DisplayPort signal detection and the Lane Swap/AUX polarity inversion logic, the CH7219 supports USB Type-C cable plug orientation switch. With internal HDCP key Integrated, the device support HDCP 1.4 and 2.3 specifications. In the device's receiver block, which supports four DisplayPort Main Link Lanes input with data rate running at 1.62Gbps, 2.7Gbps, 5.4Gbps or 8.1Gbps, and converted the input signal to HDMI output up to 4Kx2k@60Hz. Leveraging the USB Power Delivery control logic, the USB billboard module for USB device indentify and DisplayPort's unique source/sink "Link Training" routine, the CH7219 is capable of instantly bring up the video display to the HDMI/DVI TV/Monitor when the initialization process is completed.

This application note focuses only on the basic PCB layout and design guidelines for the CH7219. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures presented in this document are based on the 68-pin QFN (8x8 mm) package of the CH7219. Please refer to the CH7219 datasheet for details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7219 should be placed as close as possible to the respective pins. The following will describe guidelines on how to connect critical pins, as well as the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimal power supply decoupling is accomplished by placing a ceramic capacitor at each of the power supply pins as shown in Figure 1. These capacitors (C1, C2, C3, C4, C6, C7, C9, C11, C12, C14, C15, C16, C17, C18, C19 C21,C23,C24,C25,C26,C27 and C28) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7219 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The CH7219 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7219 ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to Table 1 for the Ground pin assignments.

2.1.2 Power Supply Pins

There are twelve power supply pins: AVCC, DVDD, AVDDPLL, VDDS, AVDD and VDDPLL. Refer to Table 1 for the Power supply pin assignments. Refer to Figure 1 for Power Supply Decoupling.

Table 1: Power Supply Pin Assignments for the CH7219

Pin	# of Pins	Type	Symbol	Description
2, 25, 41, 55	4	Power	AVCC	Analog supply voltage (3.3V)
11, 42	2	Power	DVDD	Digital supply voltage (1.2V)
18	1	Power	AVDDPLL	PLL supply voltage (1.2V)
21, 29	2	Power	VDDS	Serializer supply voltage (1.2V)
58, 59,65,66	4	Power	AVDD	Analog supply voltage (1.2V)
1	1	power	VDDPLL	Analog supply voltage (1.2V)
12, 22, 28, 43, 62 Thermal pad	6	Ground	GND	Power ground

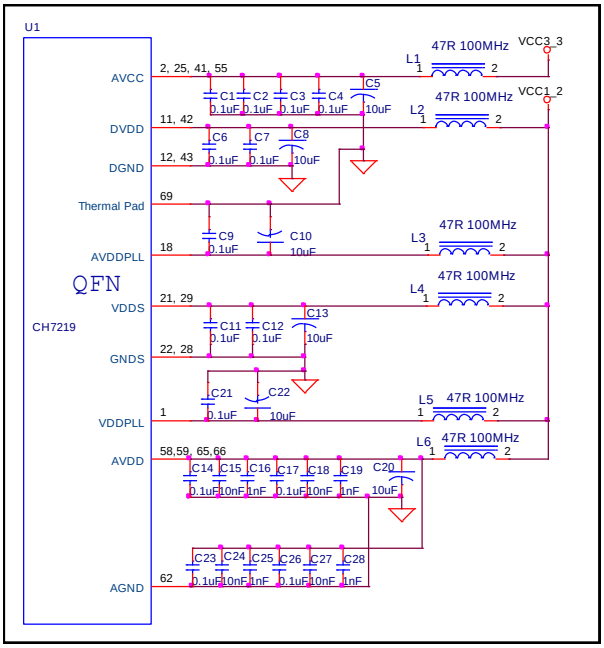

Figure 1: Power Supply Decoupling and Distribution

Note: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ωat 100MHz. Refer to Fair Rite part #2743019447 for details (an equivalent part can be used for the diagram).

2.1.3 On chip power-on reset function's sequence

The power supply must be valid and stable at least 9ms before RB signal become invalid.

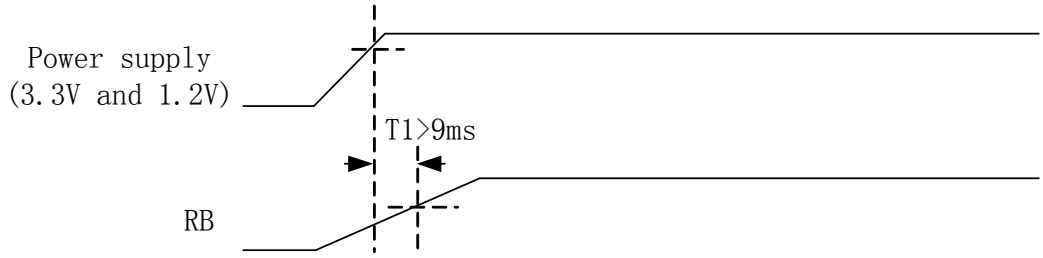

Figure 2: Power on and RB timing

2.2 Internal Reference Pins

• RBIAS pin

This pin sets the reference current for internal circuit. A 1 KΩ, 1% tolerance resistor should be connected between RBIAS and GND as shown in **Figure 3**. The distance between the resistor and the CH7219 should be less than 6mm, the shorter and wider trace the better. For optimal performance, this signal should not overlay the analog power or analog output signals.

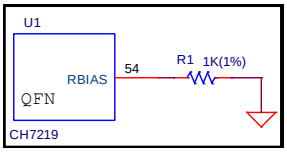

Figure 3: RBIAS Pin Connection

2.3 General Control Pins

• RB

This pin is the chip reset pin for the CH7219. The RB pin is internally pulled-up. But when it is pulled-low, this pin places the device in the power-on-reset condition.

The RB signal can be generated by on board Resistor and Capacitor delay, as shown in **Figure 5**, one 1MΩ resistor is necessary to be pulled high to 3.3V. One 0.1uf capacitor is recommended to be pulled low to GND. After the powers are stable, RB signal (low to high) is generated and sent to the chip, as shown in **Figure 2**.

While RB signal is generated by system global reset. In this case, the power supply should be valid and stable for at least 20ms before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. Otherwise, the chip can't work well. The timing is shown in **Figure 4.**

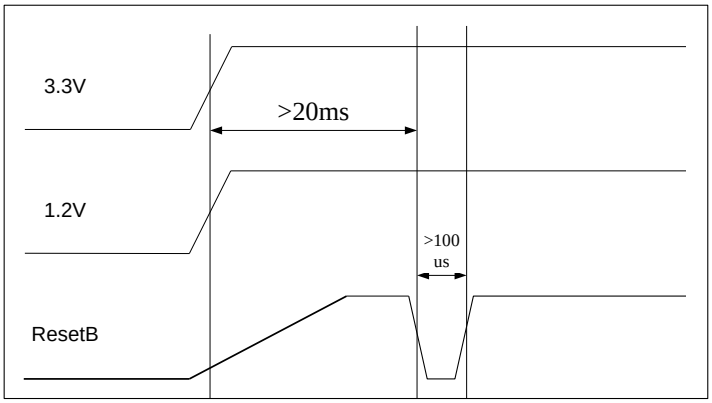

Figure 4: Power-on Reset Function's Sequence external global reset

Note:

1. The rising threshold of RB is 2.4V.
2. The falling threshold of RB is 0.4V.

• XI, XO

A 25MHz crystal (±30ppm) can be connected to XI and XO as the CH7219 the optional reference clock input. In PCB design, a 25MHz crystal must be placed as close as possible to the XI and XO pins, with traces connected from

point to point, overlaying the ground plane. Since the crystal generates the timing reference for the CH7219, it is essential that noise not couple into these input pins.

The crystal load capacitance, CL, is usually specified in the crystal spec from the vendor. Refer to **Figure 5** for a crystal circuit reference design and an example of load capacitors.

• GPIO0~8

General Purpose Input/Output Interface

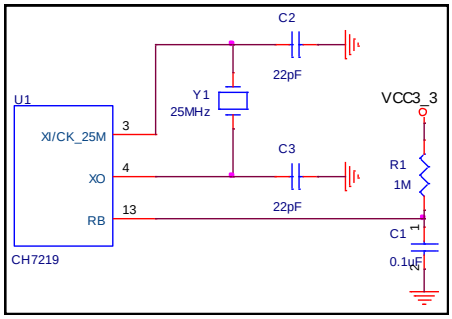

Figure 5: General Control Pins

2.4 Serial Port Control Pins

• SPC0 and SPD0

SPD0 and SPC0 function as a serial interface where SPD0 is the bi-directional data and SPC0 is an input-only serial clock. In the reference design, SPD0 and SPC0 pins are pulled up to +3.3V with 6.8k resistors. Through these two pins, the internal register values of the chip can be read.

• DDC_SC and DDC_SD

DDC_SC and DDC_SD are used to interface with the DDC of DVI/HDMI receiver. This DDC pair needs to be pulled up to 5V through 1.8 KΩ resistors

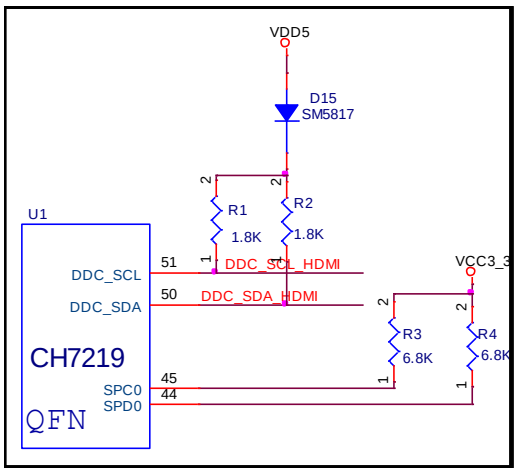

Figure 6: Serial Port Interface

2.5 Display Port Signal Pins

• DP0P/N, DP1P/N, DP2P/N, DP3P/N

These pins accept two AC-coupled differential pair signals from the Display Port transmitter or the Type-C DP Alt. For USB Type-C Receptacle application, DP Main link lane swap is supported for compliance with the USB type C cable plug orientation switch.

Since the digital serial data of the CH7219 may be toggled at speeds up to 8.1 Gbps, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7219 be kept as short as possible, avoid discontinuities in the reference plane and be isolated as much as possible from the analog outputs and analog circuitry. For optimal performance, these signals should not overlay the analog power or analog output signals. When a signal pair has to changes layers, the ground stitching vias should be placed close to the signal vias. A minimum of 1 to 3 stitching vias per pair of signals is recommended. Never route a trace so that it straddles a plane split. It is recommended that 5 mils traces be used in routing these signals. There should be 7 mils spacing between each intra pair. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 50mils. Bend smaller than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH, as shown in Figure 7.

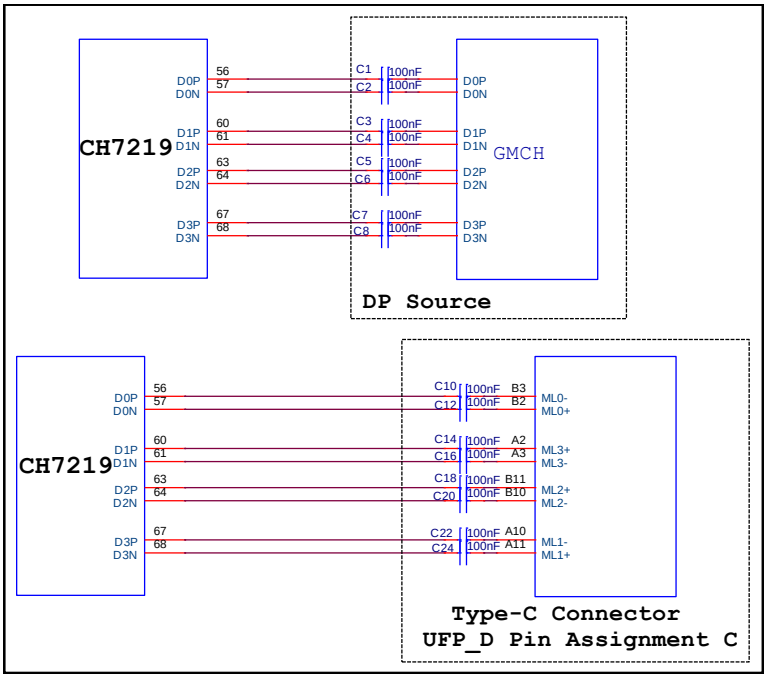

Figure 7: CH7219 DP Main Link Lane or USB Type-C DP Alt Mode Inputs

• AUXP and AUXN

These two pins are for Display Port AUX channel control or USB Type-C DP Alt Mode that accepts a half-duplex, bi-directional AC-coupled differential signal. An AC coupling capacitor, 0.1µF recommended, must be placed on the end as shown in Figure 8.

• HPD_DP

This output pin indicates whether the device is active or not. It also generates an interrupt pulse as defined by the Display Port standard. Output voltage is 3.3V. A resistor, greater than 100KΩ, should be connected between this pin and GND as shown in Figure 8.

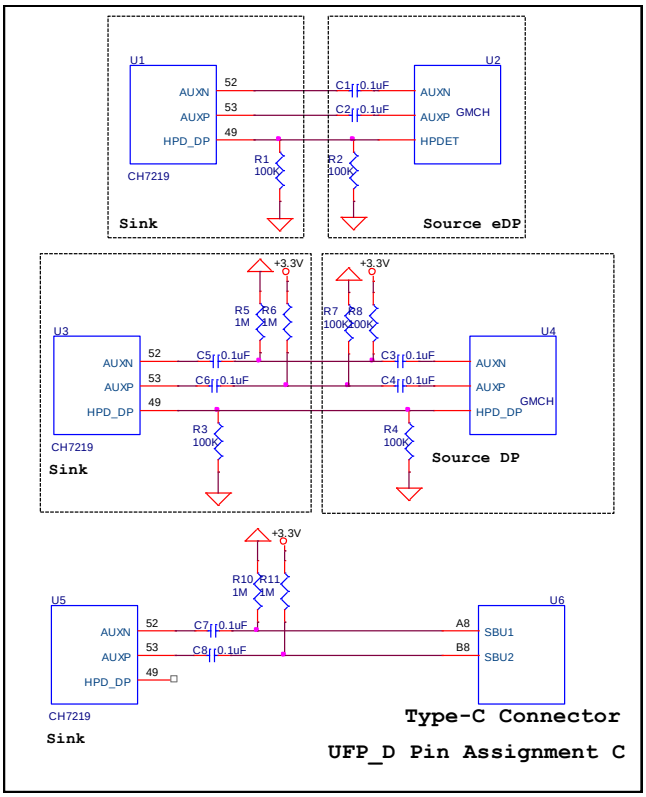

Figure 8: CH7219 AUX channel and HPD_DP

2.6 USB Type-C Signal Pins

• USB0_DN/P

The D+/- input of USB Type-C interface. These pin should be pulled low with 10K Ω or shorted to Ground directly if unused.

• VBUS_DET

Voltage input 0~5V.

• Rd

USB Type-C Dead Battery Rd Resistor, Connect CC0_A or CC1_A to this pin to enable dead battery Rd on CC0_A or CC1_A pin. It can be left open or pulled down to the ground if unused.

• CC0_A/VCONN/VCONN_DET

CC0_A Port A USB Type-C Configure Channel 0.

VCONN Connect this pin to VCONN pin of USB Type-C Plug Connector if CH7219 is used in VCONN Power Accessory mode.

VCONN_DET USB VCONN Voltage Detection, Voltage input 2.7 ~ 5.5v

• Ra

Ra Resistor. When used in typeC accessory mode, this pin needs connect to CC0. It can be left open or pulled down to the ground if unused.

• CC1_A

Port A USB Type-C Configure Channel 1

• GPIO5/CC0_B

General Purpose Input/output or Port B USB Type-C Configure Channel 0

• GPIO4/CC1_B

General Purpose Input/output or Port B USB Type-C Configure Channel 1

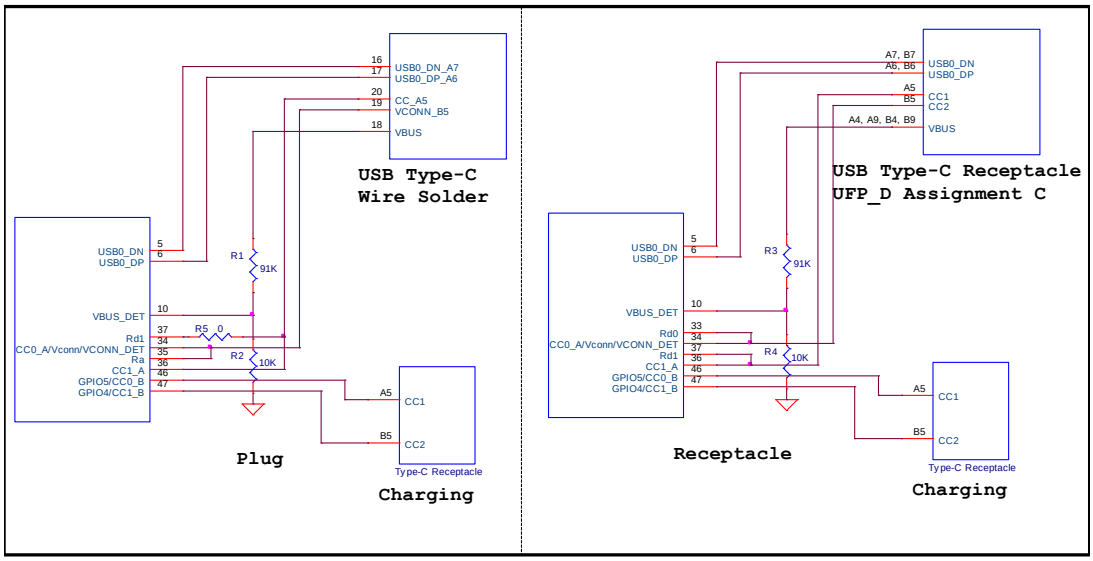

Figure 9: CH7219 Plug and Receptacle Interface

2.7 HDMI Output

The TXCB/TXC, TX0B/TX0, TX1B/TX1, TX2B/TX2 signals are high frequency differential signals that need to be routed with special precautions. Since those signals are differential, they must be routed in pairs.

2.7.1 Differential Pair Impedance

To match the external cable impedance and maintain the maximal energy efficiency it is important to meet the impedance target of 100Ω ± 10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thicknes s, board dielectric, etc. The HDMI differential pairs should be routed on the top layer directly to the HDMI connector pads if possible.

2.7.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized; inductive effects may be introduced, causing spikes in the signals. The CH7219 should be as close to the HDMI connector as possible.

2.7.3 Length Matching for Differential Pairs

The HDMI specifies the intra-pair skew and the inter-pair skew as in **Table 2**. The intra-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between the true and complement signals. The inter-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between any two single-ended data signals that do not constitute a differential pair.

Table 2: Maximum Skews for the HDMI Transmitter

Skew Type	Maximum at Transmitter
Intra-Pair Skew	0.15 T_{bit}
Inter-Pair Skew	0.20 T_{Pixel}

Where T_{bit} is defined as the reciprocal of Data Transfer Rate and T_{Pixel} is defined as the reciprocal of Clock Rate. Therefore, T_{Pixels} is 10 times T_{bit}. In other words, the intra-pair length matching is much more stringent than the inter-pair length matching.

It is recommended that length matching of both signals of a differential pair be within 5 mils. Length matching should occur on a segment-by-segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 100 mils.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

2.7.4 ESD Protection for HDMI Interface

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each HDMI output (data and clock).

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel recommended diode protection circuitry, using SEMTECH Rclamp0524P diode array devices, will protect the CH7219 device from HDMI transmitter discharges of greater than 19kV (contact) and 20kV (air). The Rclamp0524P have a typical capacitance of only 0.30pF between I/O pins. This low capacitance won't bring too much bad effect on HDMI eye diagram test.

Figure 10 show the connection of HDMI connectors, including the recommended design of Rclamp0524P diode array devices. HDMI connector is used to connect the CH7219 HDMI outputs.

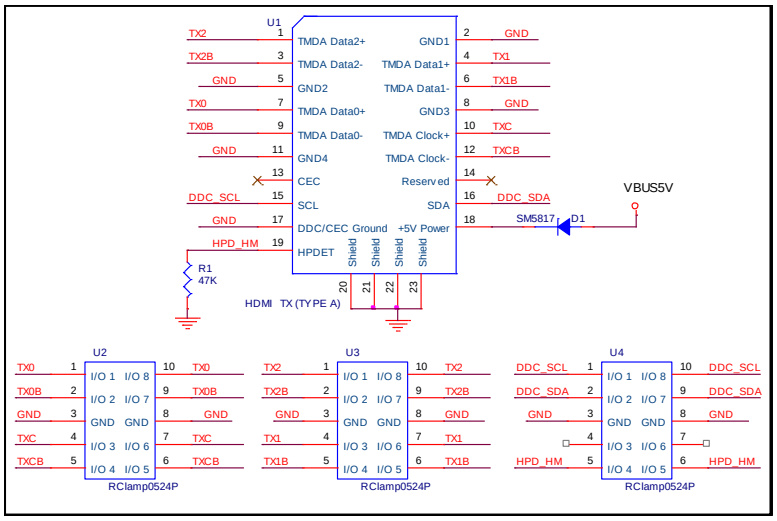

Figure 10: The connection of the HDMI outputs

• HPD_HM

This output pin connects to the GND through a 47KΩ resistor. Refer to **Figure 10** for the design example.

2.8 Thermal Exposed Pad Package

The CH7219 is available in a 68-pin QFN package with exposed thermal pad. The advantage of the exposed thermal pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed thermal pad package provides a means of reducing the thermal resistance of the CH7219. Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed thermal pad of the package should be soldered to the PCB as shown in **Figure 11**.

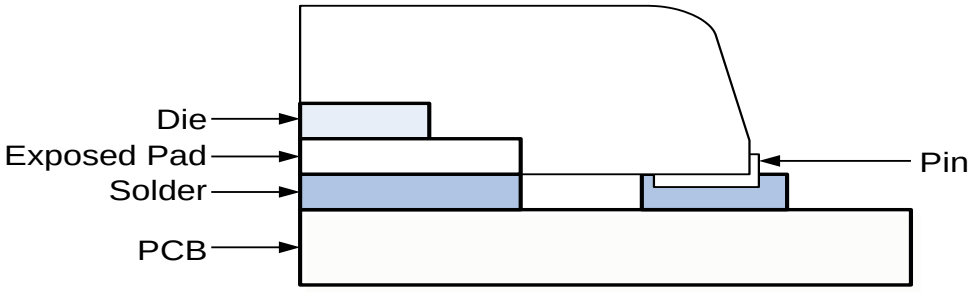

Figure 11: Cross-section of exposed thermal pad package

3.0 REFERENCE DESIGN EXAMPLE

The following schematics are to be used as a CH7219 PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7219 and would like to have a complete reference design schematic should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example

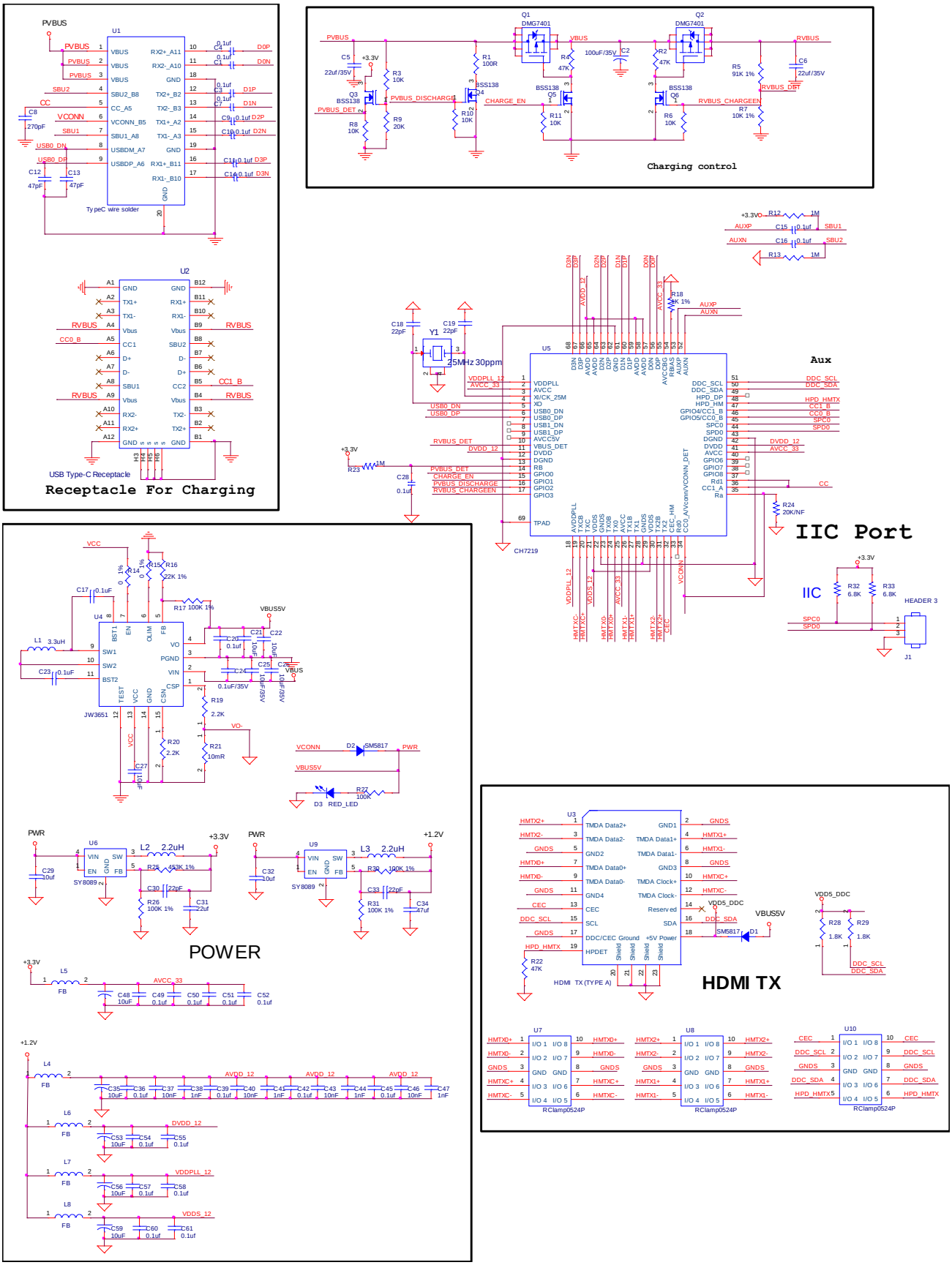

Figure 12: CH7219 Plug 1 to 2 Reference schematic

3.2 Reference Board Preliminary BOM

Table 3: CH7219 Reference Design BOM List

Item	Quantity	Reference	Part
1	28	C1,C3,C4,C7,C9,C10,C11, C14,C15,C16,C17,C20, C23,C28,C36,C39,C42,C45,C49,C50,C51,C52,C54, C55,C57, C58,C60,C61	0.1uF
2	1	C2	100uF/35V
3	2	C5,C6	22uf/35V
4	1	C8	270pF
5	2	C12,C13	47pF
6	4	C18,C19,C30,C33	22pF
7	10	C21,C22,C27,C29,C32,C35, C48,C53,C56,C59	10uF
8	1	C24	0.1uF/35V
9	2	C25,C26	10uF/35V
10	1	C31	22uf
11	1	C34	47uf
12	4	C37,C40,C43,C46	10nF
13	4	C38,C41,C44,C47	1nF
14	2	D1,D2	SM5817
15	1	D3	RED_LED
16	1	J1	HEADER 3
17	1	L1	3.3uH
18	2	L2,L3	2.2uH
19	5	L4,L5,L6,L7,L8	FB
20	2	Q1,Q2	DMG7401
21	4	Q3,Q4,Q5,Q6	BSS138
22	1	R1	100R
23	3	R2,R4,R22	47K
24	5	R3,R6,R8,R10,R11	10K
25	1	R5	91K 1%
26	1	R7	10K 1%
27	1	R9	20K
28	3	R12,R13,R23	1M
29	2	R14,R15	0 1%
30	1	R16	22K 1%
31	4	R17,R26,R30,R31	100K 1%
32	1	R18	1K 1%
33	2	R19,R20	2.2K
34	1	R21	10mR
35	1	R24	20K/NF
36	1	R25	453K 1%
37	1	R27	100K
38	2	R28,R29	1.8K
39	2	R32,R33	6.8K

40	1	U1	TypeC wire solder
41	1	U2	USB Type-C Receptacle
42	1	U3	HDMI TX (TYPE A)
43	1	U4	JW3651
44	1	U5	CH7219
45	2	U6,U9	SY8089
46	3	U7,U8,U10	RClamp0524P
47	1	Y1	25MHz 30ppm

4.0 REVISION HISTORY

Table 4: Revisions

Rev. #	Date	Section	Description
0.1	10/25/2023	All	Layout Guide and Design Guide for CH7219 release.

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www.chrontel.com

E-mail: sales@chrontel.com