Chrontel

AN-74

Application Notes

PCB Layout and Design Considerations for the CH7307C SDVO DVI Transmitter

1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7307C DVI Output Device with SDVO inputs. SDVO is a digital video interface developed by Intel. Guidelines in component placement, power supply decoupling, grounding, input signal interface and video components for the DVI link are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 48-pin LQFP package of the CH7307C. Please refer to the CH7307C datasheet for the details of the pin assignments.

2. Component Placement and Design Considerations

Components associated with the CH7307C should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor at each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C2, C3, C4, C5, C6, C7, and C8) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7307C ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7307C should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7307C ground pins should connect directly to its respective decoupling capacitor ground lead, then connect to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the ground pins assignment.

2.1.2 Power Supply Pins

Separate Digital, DVI, Analog, and DVI PLL power planes are recommended. See **Table 1** for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment of the CH7307C

Pin Assignment	# of Pins	Type	Symbol	Description
12, 28	2	Power	DVDD	**Digital Supply Voltage (2.5V)**
7, 30	2	Power	DGND	**Digital Ground**
15, 21	2	Power	TVDD	**DVI Transmitter Supply Voltage (3.3V)**
18, 24	2	Power	TGND	**DVI Transmitter Ground**
36, 42, 48	3	Power	AVDD	**Analog Supply Voltage (2.5V)**
31, 39, 45	3	Power	AGND	**Analog Ground**
1	1	Power	AVDD_PLL	**DVI PLL Supply Voltage (3.3V)**
6	1	Power	AGND_PLL	**DVI PLL Ground**

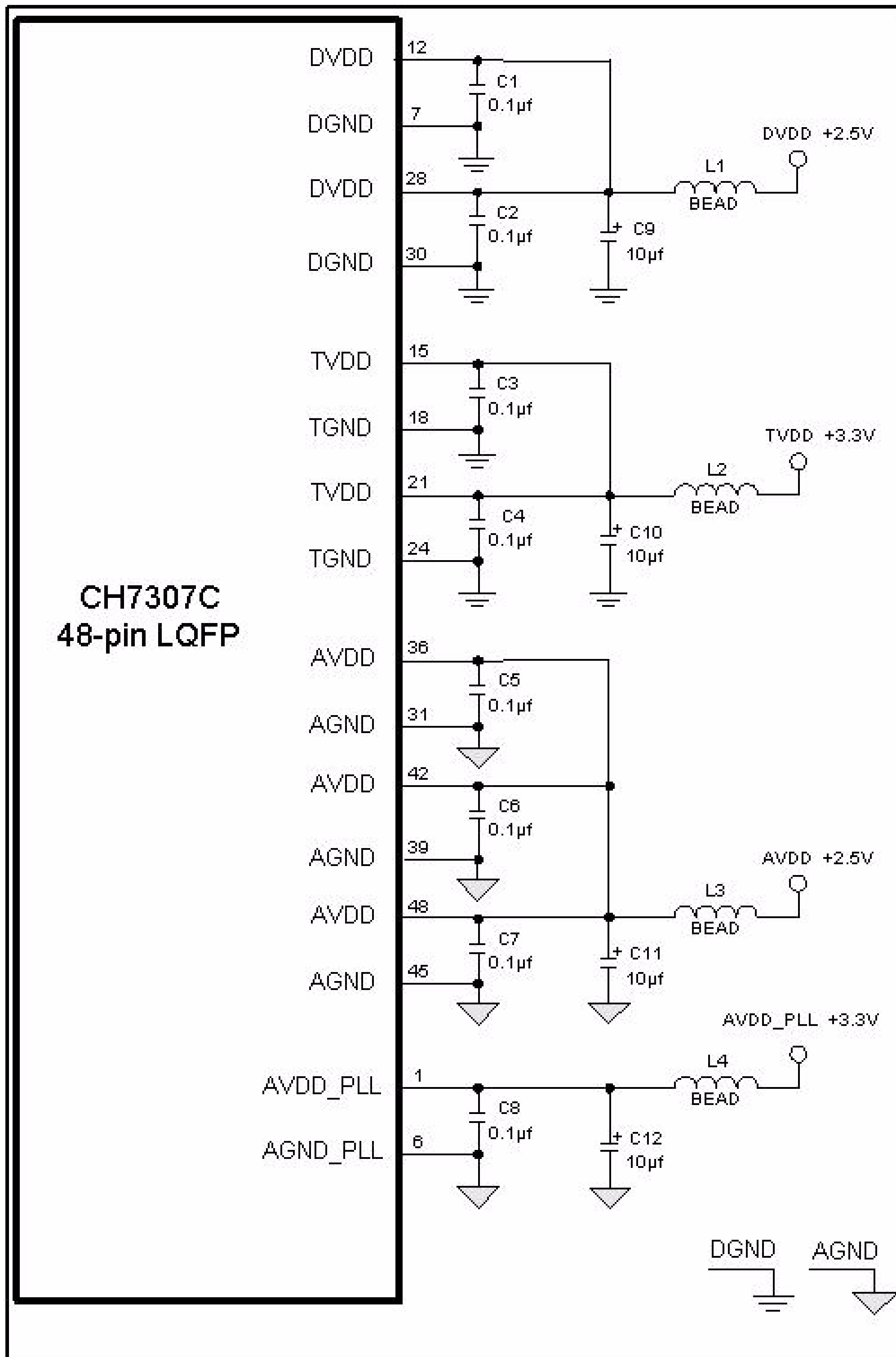


Figure 1: Power Supply Decoupling and Distribution

Notes: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Please refer to Fair_Rite part# 2743019447 for details or an equivalent part can be used for the diagram.

2.2 General Control and SDVO Signals

- **AS pin**

The Address Select pin (pin 3) can be configured as shown in **Figure 2**. This pin determines the Device Address Byte of the CH7307C. If the AS is pulled 'low', the Device Address Byte becomes 72h for serial port Write and 73h for serial port Read. If AS is pulled 'high', the Device Address Byte is 70h for serial port Write and 71h for serial port Read.

Note: When using the Intel® driver for the CH7307C, the AS pin must be pulled 'high' for a single chip design. For a dual CH7307C design, the AS pin of the primary or default CH7307C should be pulled 'high' and the AS pin of the secondary CH7307C should be pulled 'low'.

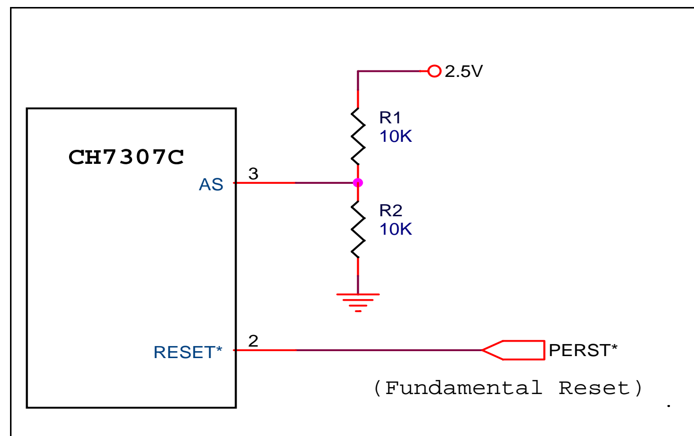


Figure 2: AS pin and RESET* pin connection

- **RESET* pin**

The RESET* pin should be connected to the Fundamental Reset of the GMCH as shown in **Figure 2**. When this pin is pulled 'low', the device is held in the power-on reset condition. When this pin is high, the reset of the device is controlled through the serial port.

- **Serial Video Inputs**

(SDVO_CLK-, SDVO_CLK+, SDVO_R-, SDVO_R+, SDVO_G-, SDVO_G+, SDVO_B-, SDVO_B+)

Since the digital serial data of the CH7307C may toggle at speeds up to 2GHz (depending on input clock speed), it is strongly recommended that the connection of these video signals between the graphics controller and the CH7307C be kept short (maximum 4 inches from edge finger to the CH7307C) and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. It is recommended that 5 mil traces be used in routing these signals. There should be 7 mil spacing between each intra pair (e.g. Red+ to Red-). Spacing between inter pairs (e.g. Red to Green) should be 20 mils. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches. Bends greater than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH.

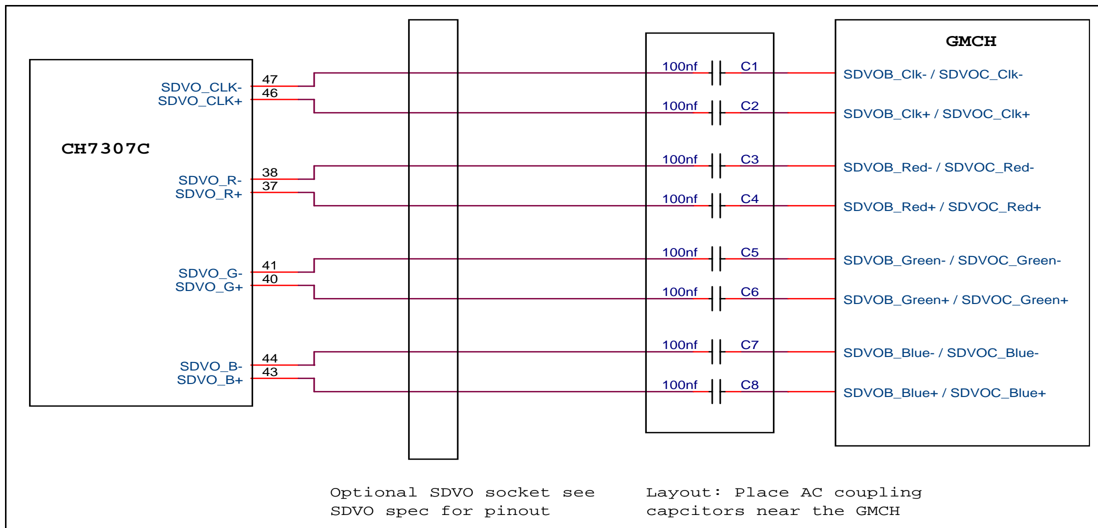


Figure 3: Differential serial video inputs

- ## SDVO_INT-, SDVO_INT+

SDVO_INT-, SDVO_INT+ is a differential output from the CH7307C. It may be used as an interrupt notification to the graphics controller. It is used to notify the graphics controller when the DVI panel hot plug detection state is changed. 100nF capacitors should be placed close to the CH7307C as AC coupling capacitors (See **Figure 4**).

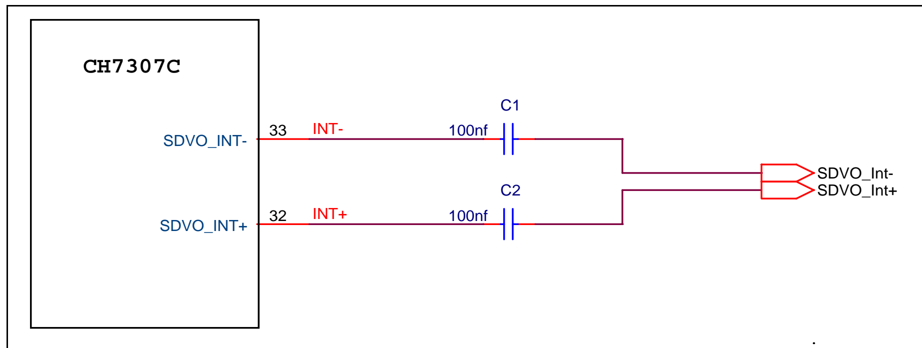


Figure 4: SDVO_INT differential pair AC coupling capacitors

- ## BSCAN

BSCAN (Pin 26) enables the boundary scan for in-circuit testing. It should be grounded with a 10K resistor in normal operation (See **Figure 5**).

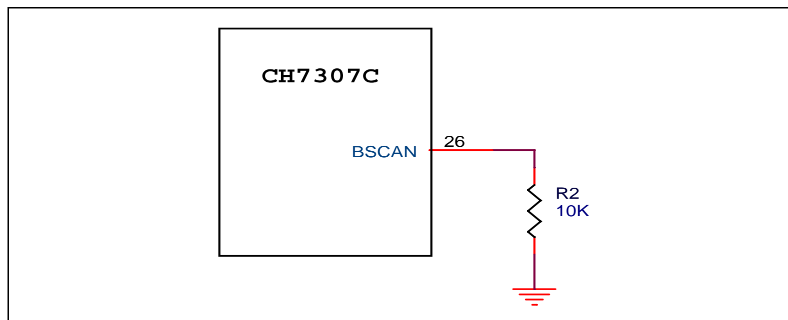


Figure 5: BSCAN strapping options

2.3 Serial Port Interface

- **SPD and SPC pins**

SPD (pin 5) and SPC (pin 4) function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 5.6 KΩ resistors (See **Figure 6**).

If the design is with Intel® Crestline chipset (Santa Rosa platform), a 56pf cap should be added from SPD line to ground to ensure a sufficient hold time for the serial data.

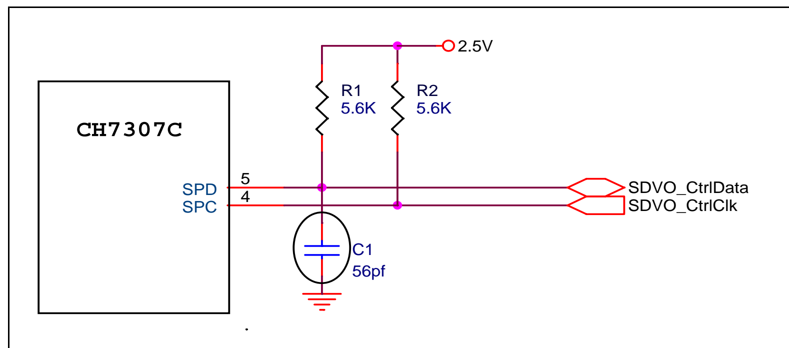


Figure 6: Serial Port Interface: SPD and SPC pins

Note: The C1 56pF cap is needed for Intel® Crestline (Santa Rosa) platform only.

- **SD_PROM and SC_PROM**

SD_PROM (pin 8) and SC_PROM (pin 9) are used to interface with the serial PROM on the ADD2* card. In the reference design, SD_PROM and SC_PROM are pulled up with 5.6 KΩ resistors (See **Figure 7**). If the design is for the motherboard-down, the PROM is not required and both SD_PROM and SC_PROM can be either pulled up or floating.

*Note: ADD2 Card: Advanced Digital Display Card - 2nd Generation. It provides digital display options for an Intel® graphics controller that supports the SDVO interface. It will not work with the graphics controller that supports Intel® DVO interface.

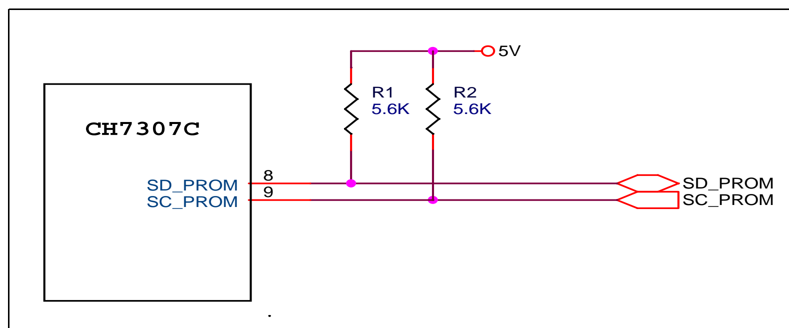


Figure 7: Serial Port Interface: SD_PROM and SC_PROM pins

- **SD_DDC and SC_DDC**

SD_DDC (pin 10) and SC_DDC (pin 11) are used to interface with the DVI monitor's DDC. In the reference design, SD_DDC and SC_DDC are pulled up with 10 KΩ resistors (See **Figure 8**).

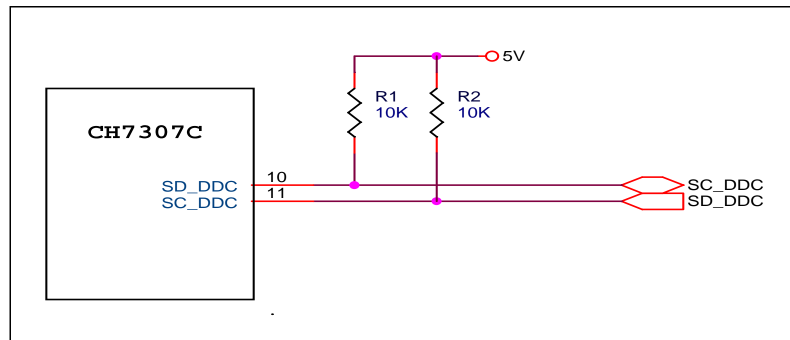


Figure 8: Serial Port Interface: SD_DDC and SC_DDC pins

2.4 CH7307C Design Options

- **Single CH7307C design**

The connection for a single CH7307C design is shown in **Figure 9**. Either SDVO port (SDVOB or SDVOC) can be used. The AS pin, pin 3, should be pulled high. The SPD EEPROM should be connected to this device.

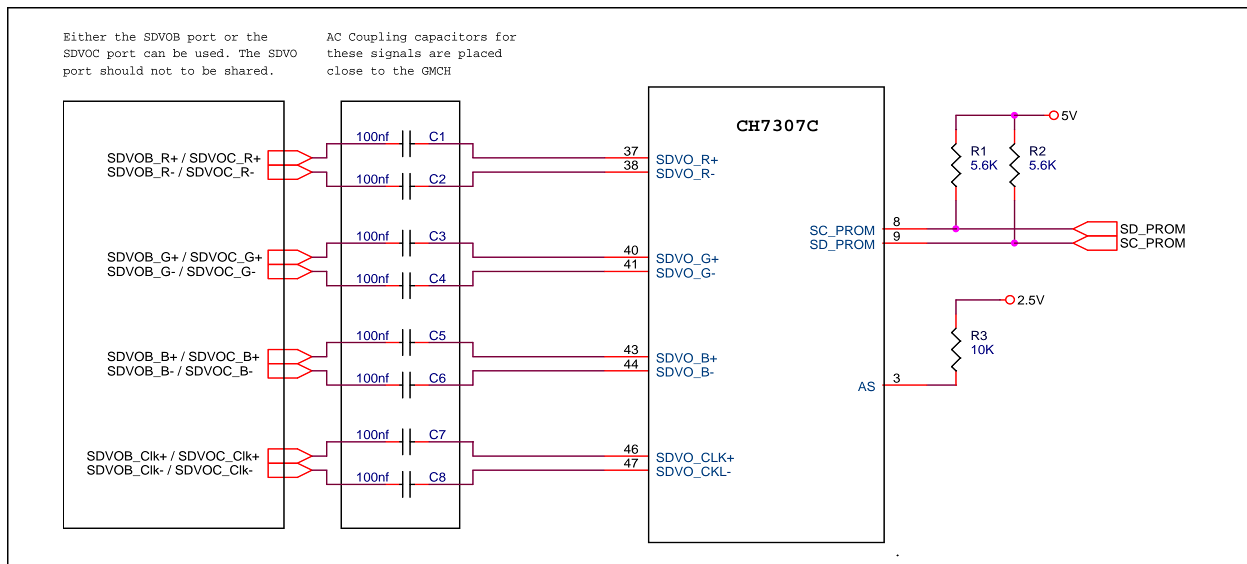


Figure 9: Single CH7307C design

- **Dual CH7307C design**

The connection for a dual CH7307C design is shown in **Figure 10**. Either SDVO port (SDVOB or SDVOC) can be used for either SDVO DVI Transmitter. The AS pin, pin 3, should be pulled 'high' for one device and 'low' for the other device. Only one SPD EEPROM is necessary and must be connected to the SDVO DVI Transmitter which has the AS pin pulled 'high'.

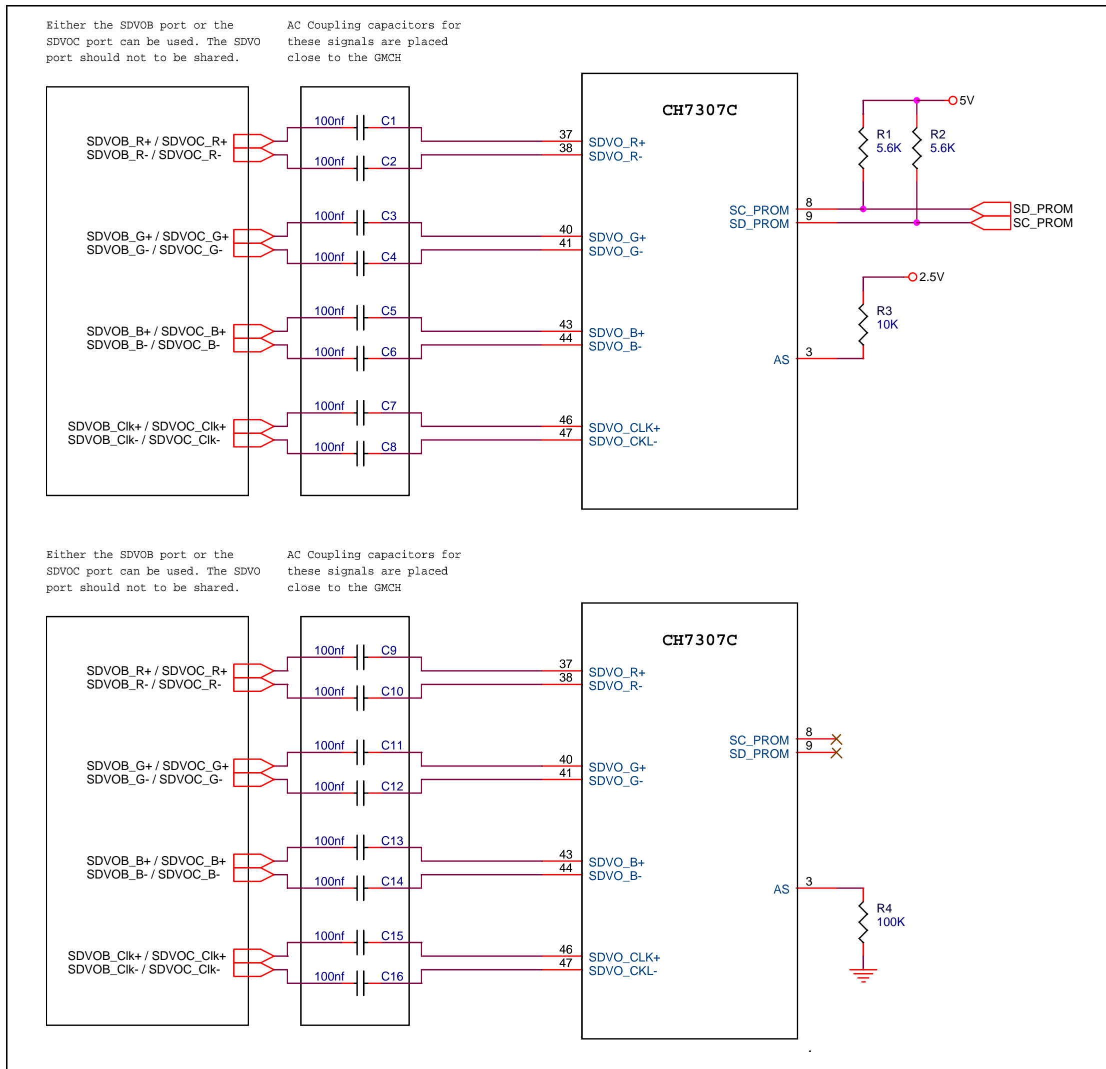


Figure 10: Dual CH7307C design

2.5 DVI Output and Control

Serialized input data, sync and clock signals are input to the CH7307C from the graphics controller's digital output port. The clock rate runs at 100MHz ~ 200MHz. The data rate is always 10 times the clock frequency. The pixel rate can be 25MP/s ~ 173MP/s. The pixel rate and the clock rate do not always equal. The clock rate can be a multiple of the pixel rate (1x, 2x or 4x depending on the pixel rate) so that the clock rate will stay in the 100MHz ~ 200MHz range. In the condition that the clock rate is running at a multiple of the pixel rate, there isn’t enough pixel data to fill the data channels. Dummy fill characters are used to stuff the data stream. For correct DVI operation, the input data format must be selected to be one of the RGB input formats.

The TDC0, TDC1, TDC2 & TLC signals are high frequency differential signals that need to be routed with special precautions. Since the TDC0, TDC1, TDC2 & TLC signals are differential they must be routed in pairs: TDC0 & TDC0*, TDC1 & TDC1*, TDC2 & TDC2*, TLC & TLC* signals. The lengths of the 4 pair of signals must be kept as close as possible. The maximum length difference must not exceed 100 mils for any of the pairs relative to each other. The number of bends should be kept to 4 or less and 45 degree is the maximum corner angle. These signals should be routed on the top layer directly to the DVI connector without any vias to the bottom layer. The pin placement of the TDC0, TDC1, TDC2 & TLC signals allows for a direct route to the DVI connector. The CH7307C comes in versions able to drive a DVI display at a pixel rate of up to 173 MHz, supporting WUXGA (1920 x 1080) resolution displays.

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each DVI Output (data and clock).

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel's recommended diode protection circuitry, using Maxim diode array devices, will protect the CH7307C-DEF device from DVI panel discharges of greater than 4kV (contact) and 8kV (air).

Figure 11 shows an example of the connection of the DVI output. In the figure a DVI-I Right Angle Connector is used to interface the CH7307C DVI outputs to the monitor.

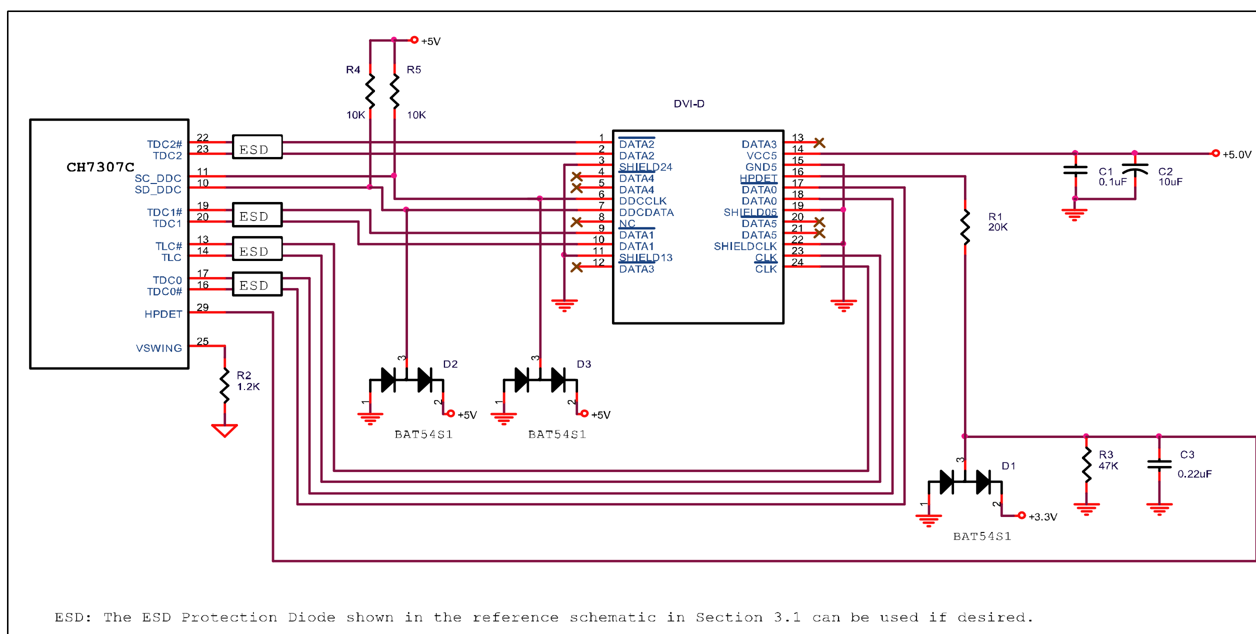


Figure 11: The connection of the DVI output

- **DVI Data Channel (TDC[2:0] and TDC[2:0]*)**

These pins (Pins 17, 20, 23 for TDC[2:0] and Pins 16, 19, 22 for TDC[2:0]*) provide the DVI differential outputs for data channel 0 (blue), channel 1(green) and channel 2 (red) (See **Figure 11**).

- **DVI Link Clock Outputs (TLC and TLC*)**

These pins (Pins 13, 14) provide the DVI differential clock outputs for the DVI interface corresponding to the data on the TDC[2:0] outputs (See **Figure 11**).

- **HPDET (DVI Hot Plug Detect)**

This input pin (Pin 29) determines whether the DVI link is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the SDVO_INT- and SDVO_INT+ (See **Figure 11**).

- **VSWING (DVI Link Swing Control)**

This pin (Pin 25) sets the swing level of the DVI outputs. A 1.2KΩ resistor should be connected between this pin and GND using short and wide traces (See **Figure 11**).

2.6 48 LQFP with Thermal Exposed Pad Package

The CH7307C is available in a 48 pin LQFP with thermal exposed pad package. The part number for this type of package is CH7307C-DE. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7307C. Simulation results show that a 4 layer PCB design with a 4mm x 4mm thermal land pad and a 3x3 via grid array has a thermal resistance (θ **ja)** of approximately 25 ^{o}C/W (see **Table 4** for details).

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 12**.

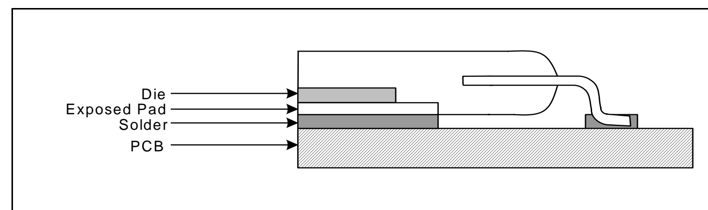


Figure 12: Cross-section of the LQFP exposed pad package

Figure 13 below shows the placement of the thermal land pattern. The thermal land pattern should have a 3x3 grid array of 1.2 mm pitch thermal vias connected to the ground layer of the PCB. These vias should be 0.3 mm in diameter with 1 oz copper via barrel plating.

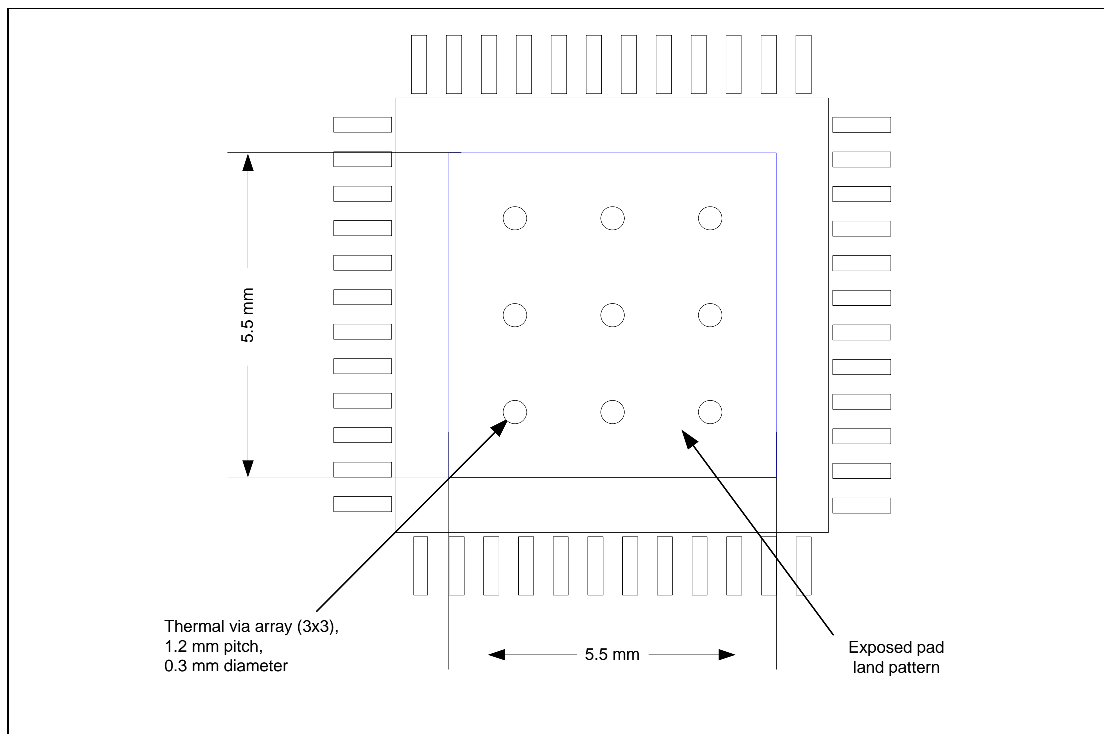


Figure 13: Thermal Land Pattern

When applying solder paste to the thermal land pattern, the recommended stencil thickness is from 5 to 8 mils. The stencil should allow solder paste to be applied in 9 paste islands as shown in **Figure 14**.

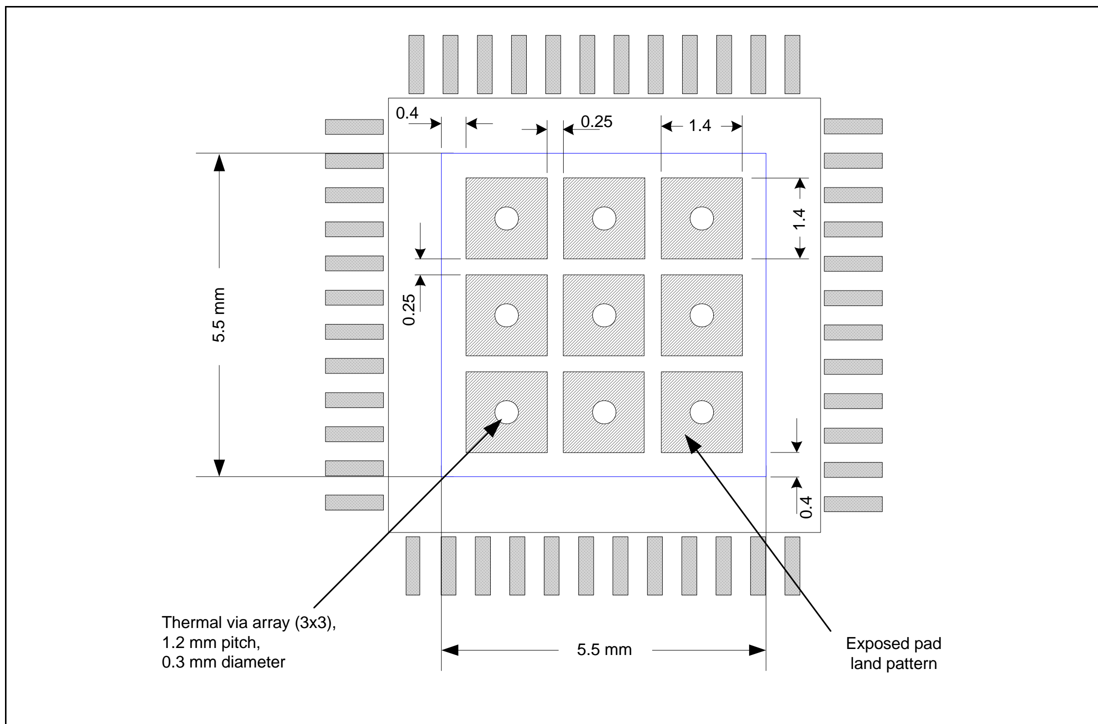


Figure 14: Solder Stencil

Thermal resistance was calculated using the thermal simulation program called ANSYS. The design conditions and material property assumptions used are shown in **Table 2** and **Table 3**.

Table 2: Package and Simulation Conditions

Package Description	
Package Type	Exposed Pad LQFP
Lead Count	48 pin
Package Size	7 mm x 7 mm
Pad Size	5.5 mm x 5.5 mm
Lead Frame Material	Cu (C7025)
PCB Description	
PCB Layers	4 Layers
PCB Dimensions	76.2 mm x 114.3 mm
PCB Thickness	1.6 mm
Simulation Conditions	
Power Dissipation	1.3 W

Table 3: Thermal Conductivity of Component Materials (lead-free)

Material	k, W/m ^{o}C
Lead Frame	172
Silicon	148 at 25 ^{o}C
	98.9 at 125 ^{o}C
Molding Compound	1.0
Copper	389
Epoxy	1.1
FR-4	0.3

Table 4: Simulation Results

# of PCB vias	θ ja (°C/W)			ψ jt (°C/W)	θ jc (°C/W)
	0 m/s	1 m/s	2 m/s		
9	25.9	22.2	21.1	2.6	30.3

Note:

θ ja:Thermal resistance from junction to ambient with 0 m/s, 1 m/s, and 2 m/s of forced air convection
ψ jt:Thermal resistance characterization parameter from junction-to-top center
θ jc:Thermal resistance from junction to case

The theoretical junction temperature of the CH7307C can be calculated using the following formula:

$T_J = T_A + \theta_{JA} * P_H$

Where T_J = Junction temperature

T_A = Ambient temperature

θ_{JA} = Thermal resistance from junction to ambient

P_H = Power dissipation

Under normal operating conditions, the CH7307C dissipates approximately 1.3 Watts of power. The recommended ambient operating temperature is between 0 °C and 70 °C. **Table 5** provides the minimum and maximum theoretical junction temperature of the CH7307C when using the PCB guidelines described in this section.

Table 5: Theoretical Junction Temperature (°C)

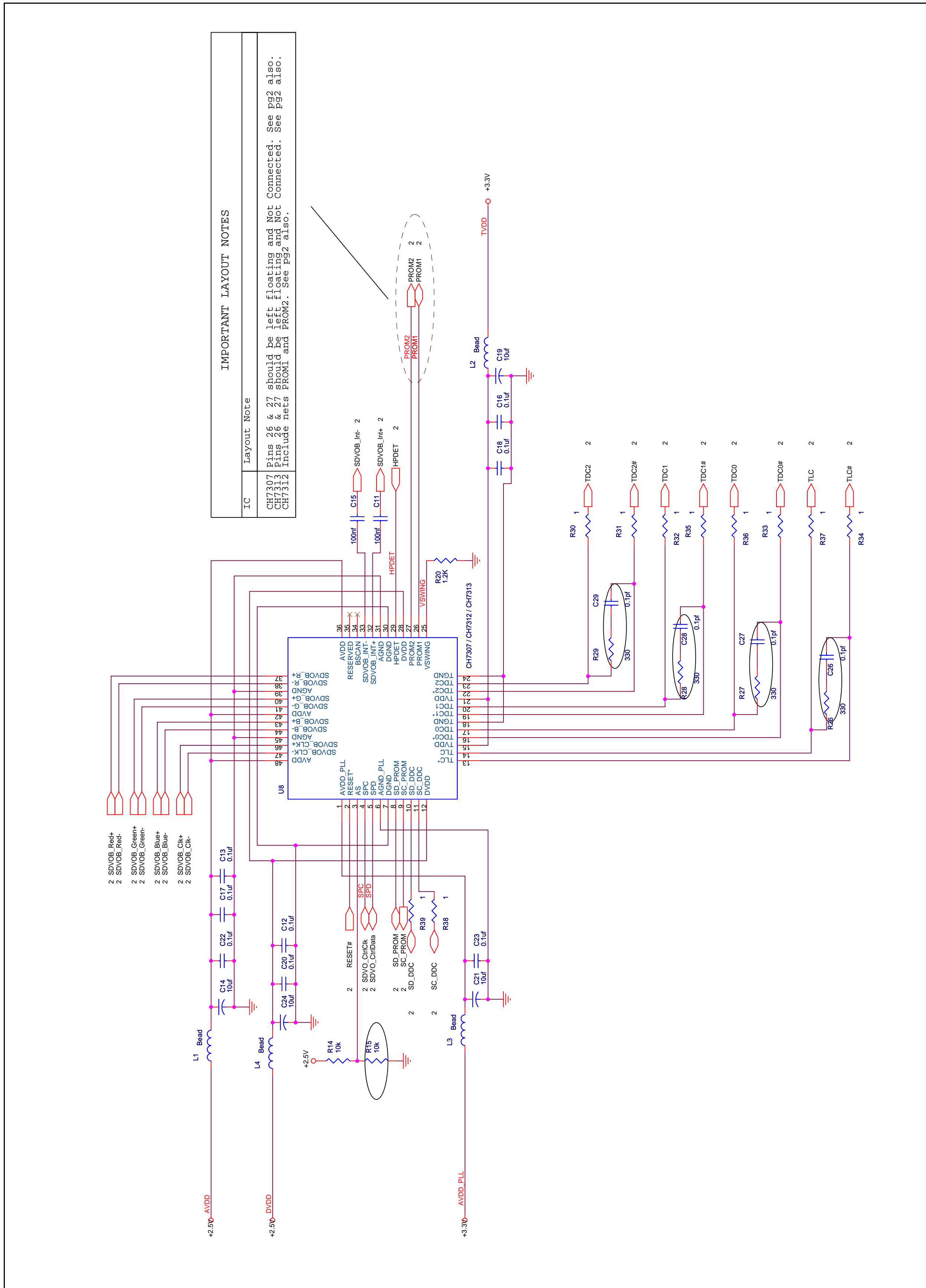
T_A°C	Forced Air Convection		
	0 m/s	1 m/s	2 m/s
0	34	29	27
70	104	99	97

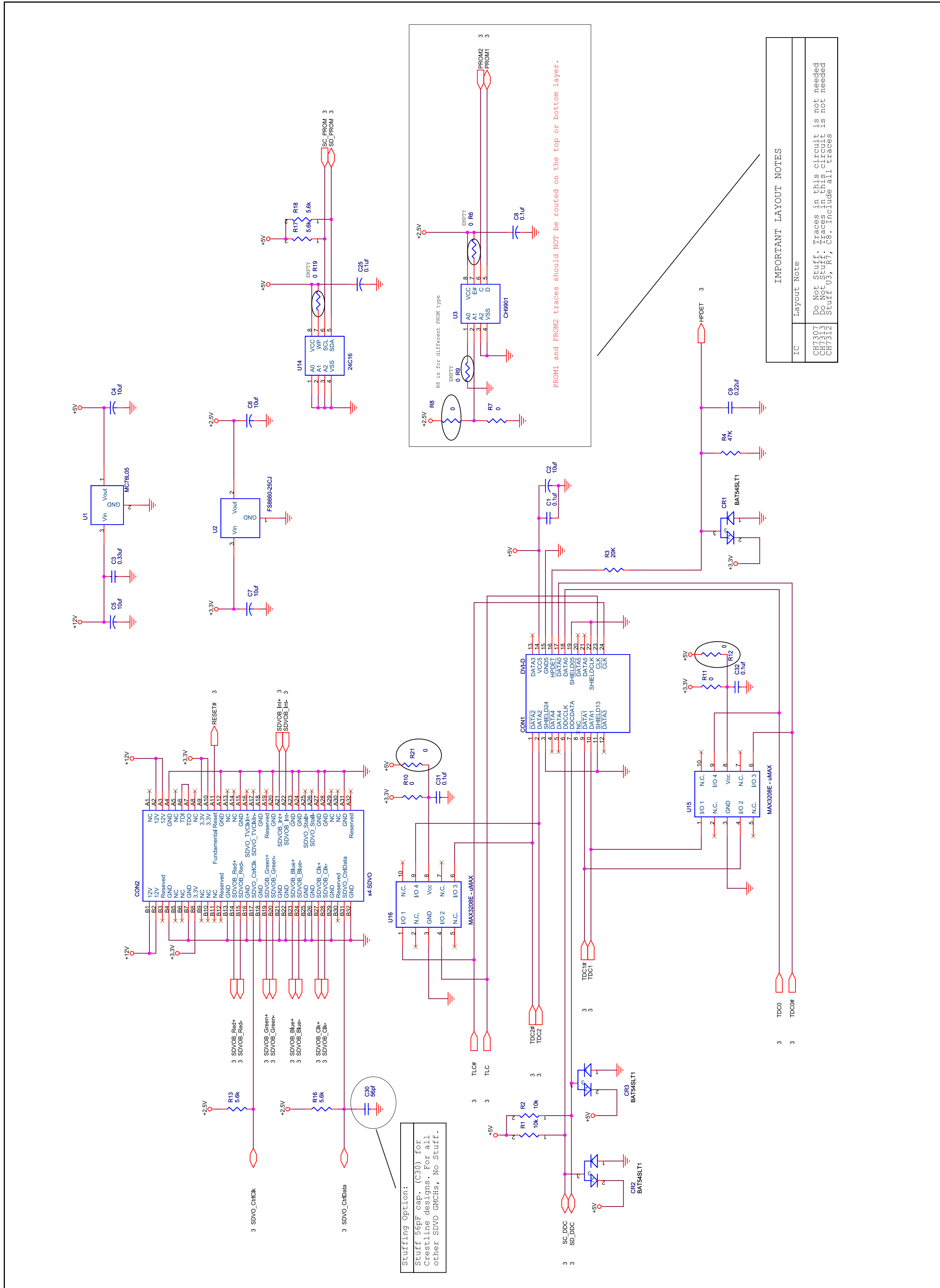
It is recommended that a thermal modeling analysis be performed specifically for each application.

3. Reference Design Example

The following schematics are based on an Intel® Grantsdale-G graphics chipset design and are to be used as a CH7307C PCB design example only. It is not a complete design. The schematic can accommodate other Chrontel DVI transmitter IC's. Layout and stuffing options for the CH7307C, as described in the schematic should be followed. Those who are seriously doing an application design with the CH7307C and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example





3.2 Evaluation Board Preliminary BOM

Item	Qty	Reference	Part	Description		Part Number
1	1	CON1	DVI-D	DVI Connector	D	WM5600-ND
2	3	CR1,CR2,CR3	DualDiode	BAT54SLT1	AV	BAT54SLT1
3	13	C1,C8,C12,C13,C16,C17,	0.1uf	CAP .1UF 16V CERAMIC Y5V 0603	D	PCC1788CT-ND
		C18,C20,C22,C23,C25,C31,				
		C32				
4	9	C2,C4,C5,C6,C7,C14,C19,	10uf	CAP 10UF 16V TANT TE SERIES	D	PSC3106TR-ND
		C21,C24				
5	1	C3	0.33uf	CAP .33UF 16V CERAMIC Y5V 0603	D	399-1291-1-ND
6	1	C9	0.22uf			
7	2	C11,C15	100nf	CAP .1UF 16V CERAMIC Y5V 0603	D	PCC1788CT-ND
8	4	C26,C27,C28,C29	0.1pf			
9	1	C30	56pf			
10	4	L1,L2,L3,L4	Bead	CHIP FERRITE 100 OHM 25% 0805 SMD	D	PMC0805-101-ND
11	4	R1,R2,R14,R15	10K	RES 10K OHM 1/10W 5% 0603 SMD	D	P10KGCT-ND
12	1	R3	20K	RES 20K OHM 1/10W 5% 0603 SMD	D	P20KGCT-ND
13	1	R4	47K	RES 47K OHM 1/10W 5% 0603 SMD	D	P47KGCT-ND
14	9	R6,R7,R8,R9,R19	0	RES 0.0 OHM 1/10W 5% 0603 SMD	D	311-0.0GCT-ND
		R10,R11,R12,R21				
15	4	R13,R16,R17,R18	5.6k	RES 5.6K OHM 1/10W 5% 0603 SMD	D	311-5.6KGCT-ND
16	1	R20	1.2K	RES 1.2K OHM 1/10W 5% 0603 SMD	D	P1.2KGCT-ND
17	4	R26,R27,R28,R29	330	RES 330 OHM 1/10W 5% 0603 SMD	D	P330GCT-ND
18	10	R30,R31,R32,R33,R34,R35,	1 ohm	RES 1.0 OHM 1/10W 5% 0603 SMD	D	P1.0GCT-ND
		R36,R37,R38,R39				
19	1	U1	MC78L05	LINEAR REGULATOR	A	MC7805ABP
20	1	U2	FS8660-25CJ			
21	1	U3	CH9901	IC, Chrontel CH9901 HDCP key	Chrontel	CH9901
22	1	U8	CH7307	IC, Chrontel CH7307 DVI Transmitter	Chrontel	CH7307
23	1	U14	24C16	ST EEPROMS SO-8SO-8 2KX8 SERIAL	M	511-M24C16-WMN6
24	2	U15,U16	MAX3208E - uMAX	IC, High Speed Differential ESD Protection IC	Mx	MAX3208EAUB

Supplie	Name	Site
D	Digikey	www.digikey.com
M	Mouser	www.mouser.com
MMD	MMD Components	www.mmdcomp.com
AV	Avnet (Kent Elect.)	www.avnet.com
A	Arrow	www.arrow.com
F	Future Electronics	www.futureelectronics.com
Mx	Maxim	www.maxim-ic.com

4. Revision History

Rev. #	Date	Section	Description
1.0	11/21/2003	All	First official release
1.21	01/27/2005	All	Update to CH7307C
1.3	10/2/2006	2.3, 2.5 & 3	Added 56pf option for Intel®Crestline design, ESD & HPDET related update.

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