Measurement of the CH7308 Panel Power Sequencing

Overview

The CH7308 conforms to the SPWG LVDS panel power sequencing requirements. T1 - T5 in Figure 1 are the SPWG LVDS panel power sequence timing parameters. These parameters can be customized through use of Intel's VBT (VBIOS Blockdata Table) utility to comply with many of the LVDS panels on the market. This Technical Bulletin describes how to verify the T1 - T5 timings.

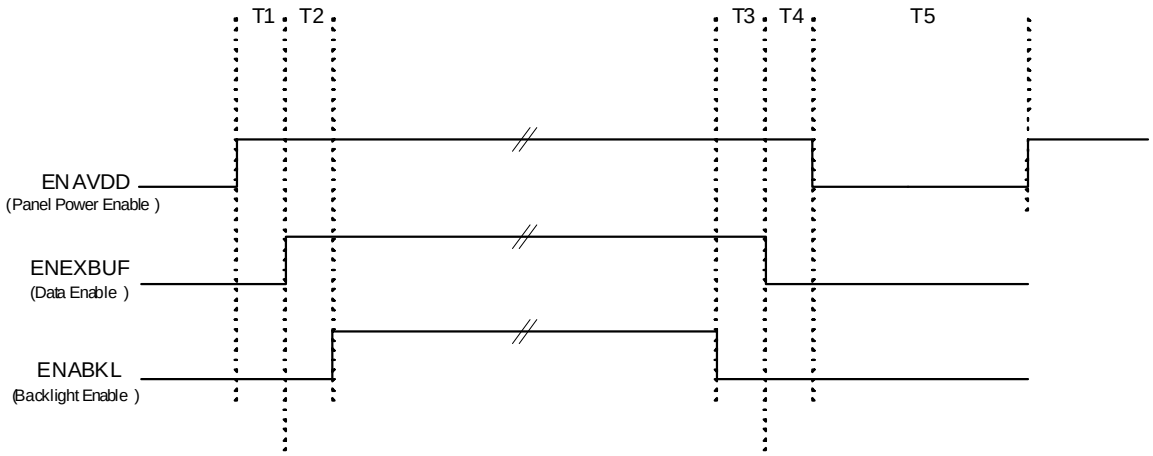

Figure 1: LVDS T1 - T5 Power Sequencing

Where T1 - T5 are defined as follows:

T1: The duration between the time the power to the panel has been turned on (ENAVDD=high) to the time valid data is allowed to be gated out (ENEXBUF=high).
T2: The period between ENEXBUF = high and the time the LVDS backlight is enabled (ENABKL=high).
T3: The time period after the back light is disabled and before the ENEXBUF signal is set to low.
T4: The time prior to ENAVDD going low after the ENEXBUF signal is set to low.
T5: The waiting time required prior to enabling power on after the power has been off.

The purpose of this technical bulletin is to help verify that the T1-T5 timings are correct and comply with the specification of the LVDS panel the CH7308 is to interface with.

Measurement of T1-T5

To measure T1-T5, we need to monitor ENAVDD (pin 2), ENABKL (pin 1), and ENEXBUF.

The ENEXBUF signal can be gated out of the TEST pin (pin 50) using a CH7308 serial port read/write utility. Please contact the Chrontel Applications Group to obtain this utility. Once obtained, write to the following registers with the values below:

Register 4Bh[1]: 0b
Register 4Ah: 0Eh

After the ENEXBUF signal is setup to output to pin 50, follow the procedure below to measure the T1-T5 timings.

1. Connect signals ENAVDD (pin 2), ENEXBUF (pin 50), and ENABKL (pin 1) to an oscilloscope.
2. Set the trigger of the oscilloscope to the probe connected to the ENAVDD signal.
3. Enable the trigger of the oscilloscope.
4. Initiate a video mode switch from one resolution to another.
5. All waveforms needed to measure the T1 - T5 parameters should now be displayed.
6. Using Figure 1 as a reference, measure T1 - T5 using the reference cursors of the oscilloscope

Figure 2 below is an example of a captured CH7308 panel power sequence with a T3 timing of 220ms.

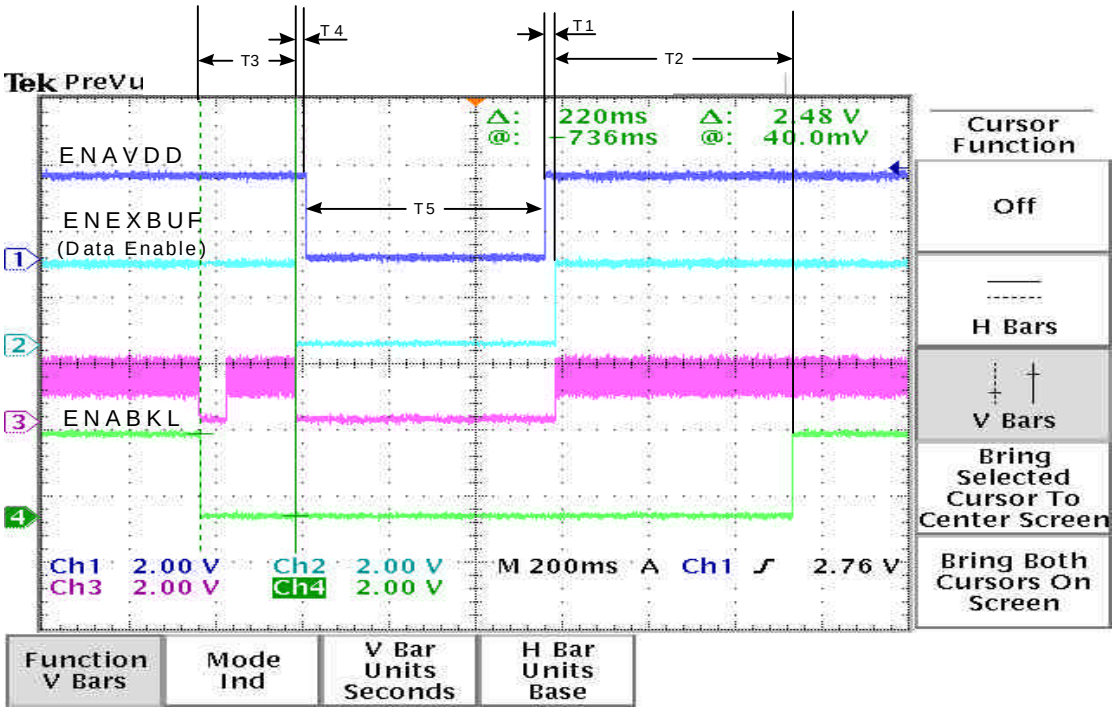

Figure 2: Power Sequence Timing Measurement Using a Tektronix Scope

Where:
signal 1 = ENAVDD (VDD Enable)
signal 2 = ENEXBUF (Data Enable)
signal 3 = LVDS Data
signal 4 = ENABKL (Backlight Enable)

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