PCB Layout and Design Considerations for CH7317B SDVO* / RGB DAC

1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7317B VGA RGB Bypass Output Device with SDVO inputs. SDVO is a digital video interface developed by Intel. Guidelines in component placement, power supply decoupling, grounding, input signal interface and VGA RGB bypass connection are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 64-pin LQFP and QFN packages of the CH7317B. Please refer to the CH7317B datasheet for the details of the pin assignments. QFN package of CH7317B has an exposed pad that should be connected to the ground of PCB.

2. Component Placement and Design Considerations

Components associated with the CH7317B should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C2, C3, C4, C5, C6, C7 and C8) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7317B ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7317B should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7317B ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

Separate Digital, DAC, Analog, and PLL power planes are recommended. See **Table 1** for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment of the CH7317B

Pin Assignment	# of Pins	Type	Symbol	Description
13, 35	2	Power	DVDD	Digital Supply Voltage (2.5V)
10, 37	2	Power	DGND	Digital Ground
16	1	Power	VDAC2	DAC Supply Voltage (3.3V)
17	1	Power	GDAC2	DAC Ground
19	1	Power	VDAC1	DAC Supply Voltage (3.3V)
23	1	Power	GDAC1	DAC Ground
27	1	Power	VDAC0	DAC Supply Voltage (3.3V)
31	1	Power	GDAC0	DAC Ground
52, 58, 64	3	Power	AVDD	Analog Supply Voltage (2.5V)
49, 55, 61	3	Power	AGND	Analog Ground

***** Intel Proprietary

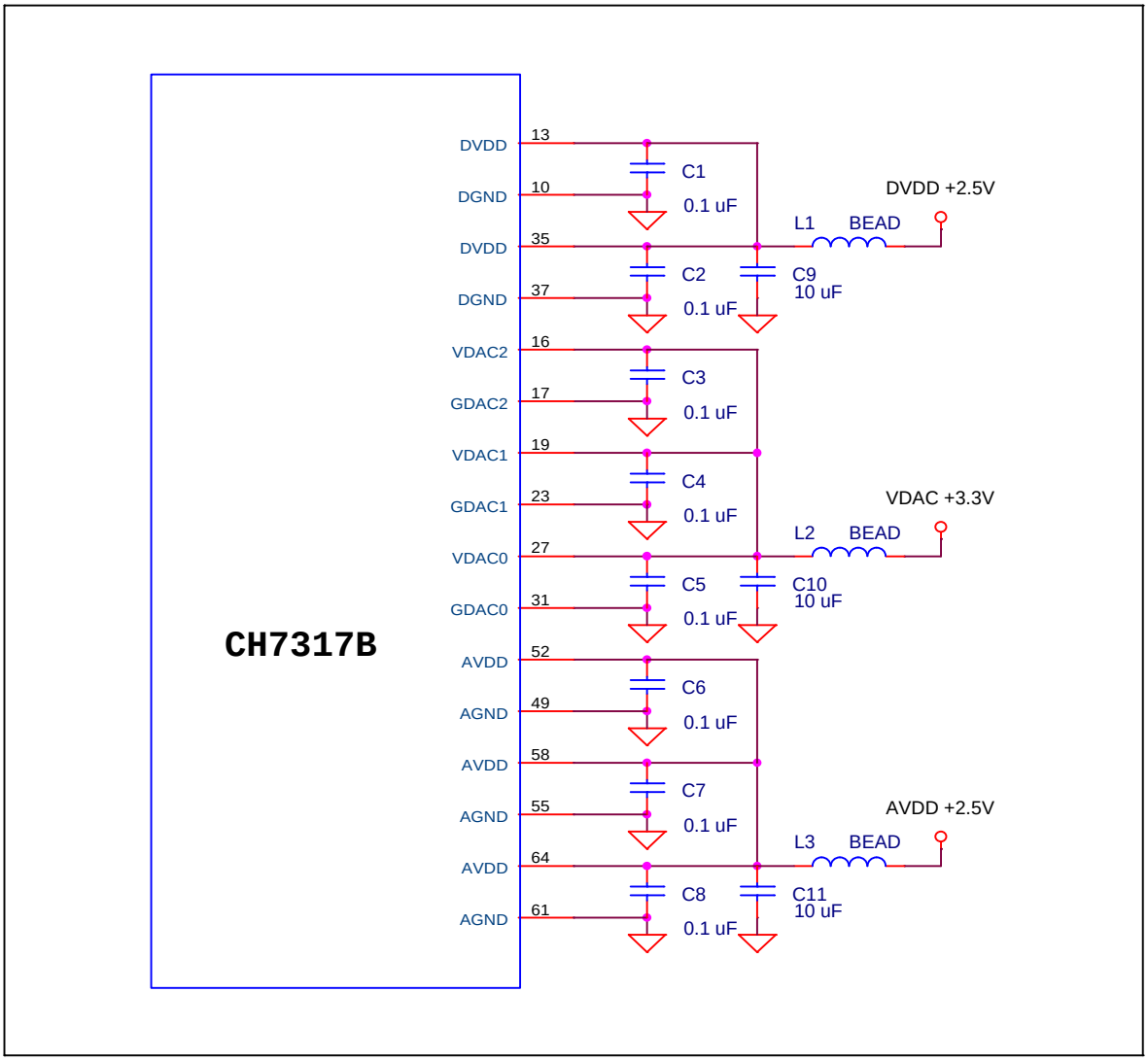

Figure 1: Power Supply Decoupling and Distribution

Notes: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Please refer to Fair_Rite part# 2743019447 for details or an equivalent part can be used for the diagram.

2.2 General Control and SDVO Signals

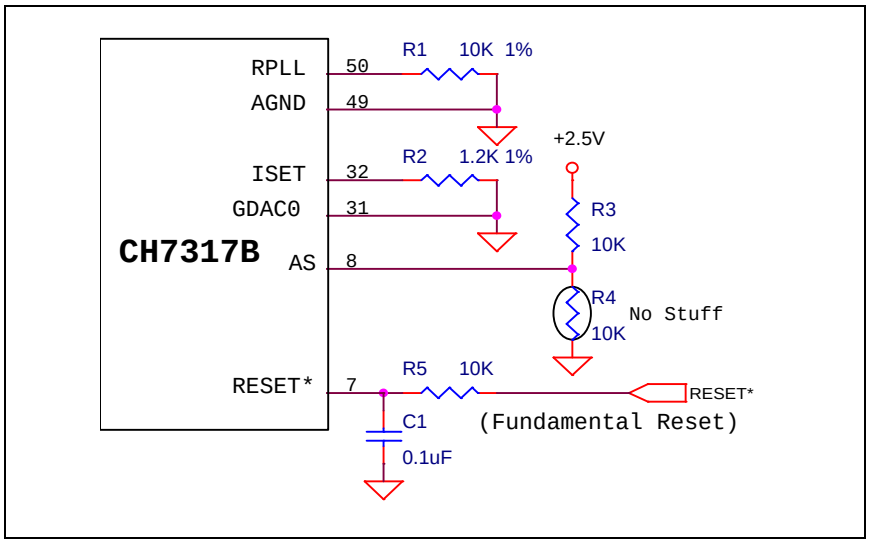

Figure 2: ISET, AS, RPLL and RESET* pin connection

- **ISET pin**

  A 1.2KΩ, 1% resistor should be connected directly between ISET (pin 32) and DAC ground (pin 31) as close as possible to the ISET pin using short and wide traces. See **Figure 2** for design reference.

- **AS pin**

  The Address Select pin, pin 8, can be configured as shown in **Figure 2**. This pin determines the serial port address of the device. If AS is pulled 'low', the serial port address is 72h. If AS is pulled 'high', then the serial port address is 70h.

- **RPLL pin**

  A 10KΩ, 1% resistor should be connected directly between RPLL (pin 50) and AGND (pin 49) as close as possible to the RPLL pin using short and wide traces. See **Figure 2** for design reference.

- **RESET* pin**

  The RESET pin should be connected to the Fundamental Reset of the GMCH as shown in **Figure 2**. When this pin is pulled 'low', the device is held in the power-on reset condition. When this pin is high, the reset of the device is controlled through the serial port.

- **Serial Video Inputs**

  (SDVO_CLK-, SDVO_CLK+, SDVO_R-, SDVO_R+, SDVO_G-, SDVO_G+, SDVO_B-, SDVO_B+)

  Since the digital serial data of the CH7317B may toggle at speeds up to 2GHz (depending on input clock speed), it is strongly recommended that the connection of these video signals between the graphics controller and the CH7317B be kept short (maximum 4 inches from edge finger to the CH7317B) and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. It is recommended that 5 mil traces be used in routing these signals. There should be 7 mil spacing between each intra pair (e.g. Red+ to Red-). Spacing between inter pairs (e.g. Red to Green) should be 20 mils. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches. Bends greater than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH.

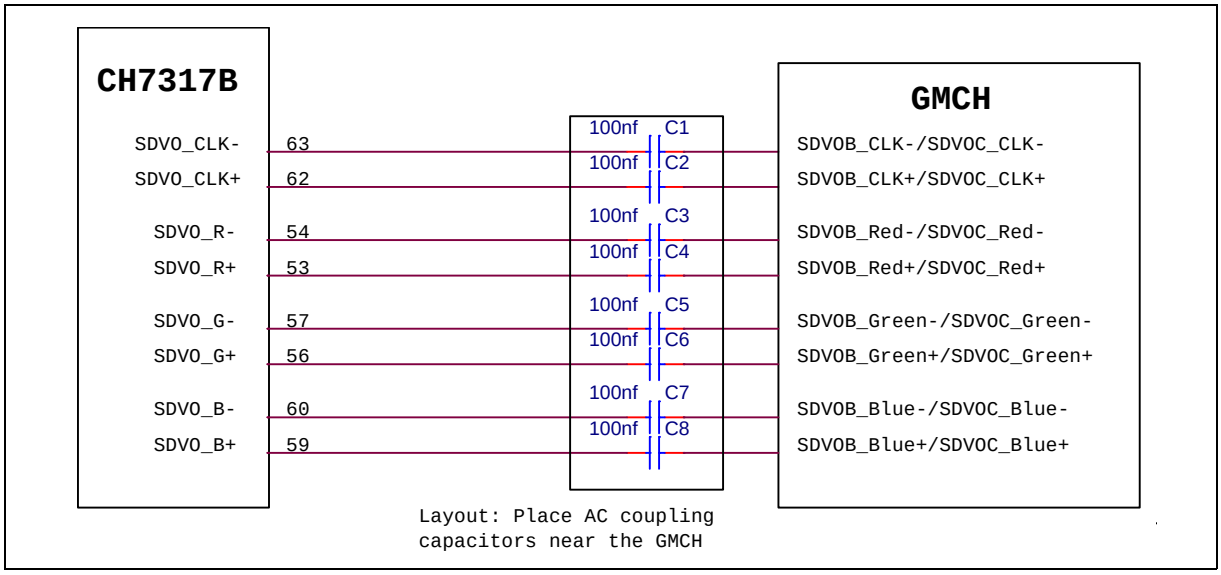

Figure 3: Differential serial video inputs

2.3 Serial Port Interface

- **SPD and SPC pins**

SPD (pin 11) and SPC (pin 12) function as a serial interface where SPD and SPC are bi-directional data and clock signals, respectively. In the reference design, SPD and SPC are pulled up with 5.6 KΩ resistors (See **Figure 4**).

If the design is with Intel Crestline chipset, a 56pF cap should be added from SPD line to ground to ensure a sufficient hold time for the serial data (See **Figure 4**).

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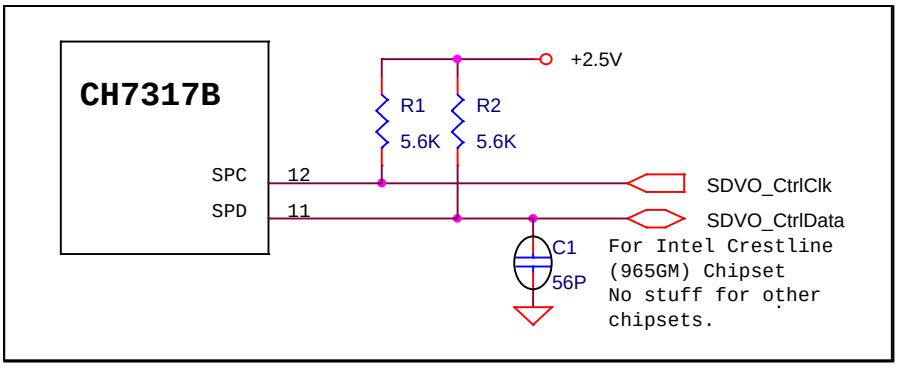


Figure 4: Serial Port Interface: SPD and SPC pins

- **SD_PROM and SC_PROM**

SD_PROM (pin 4) and SC_PROM (pin 5) are used to interface with the serial PROM on the ADD2† card. In the reference design, SD_PROM and SC_PROM are pulled up with 5.6 KΩ resistors (See **Figure 5**). If the design is on the motherboard-down, the PROM is not required and both SD_PROM and SC_PROM can be either pulled up or floating.

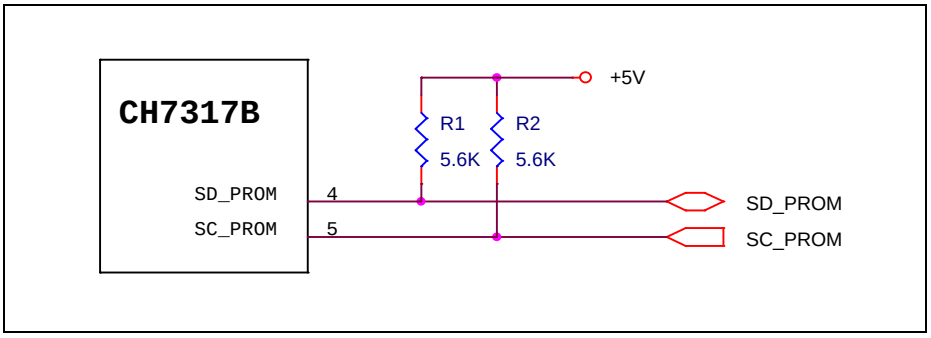


Figure 5: Serial Port Interface: SD_PROM and SC_PROM pins

- **SD_DDC and SC_DDC**

SD_DDC (pin 2) and SC_DDC (pin 3) are used to interface with the VGA monitor's DDC lines. In the reference design, SD_DDC and SC_DDC are pulled up with 10 KΩ resistors to +5V. (See **Figure 6**).

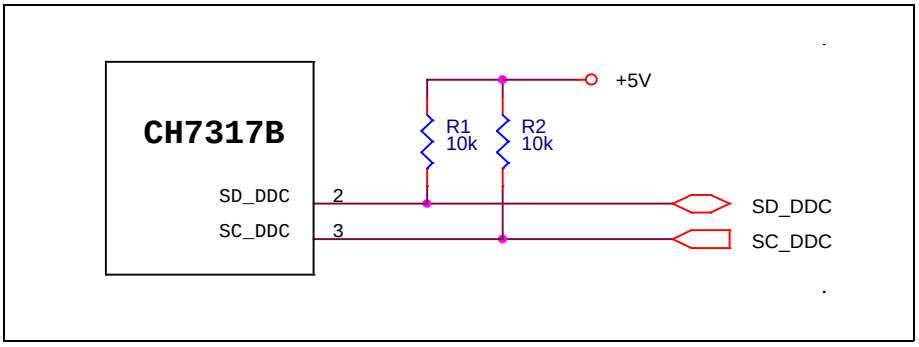


Figure 6: Serial Port Interface: SD_DDC and SC_DDC pins

† Note: ADD2 Card: Advanced Digital Display Card - 2nd Generation. It provides digital display options for an Intel® graphics controller that supports the SDVO interface. It will not work with the graphics controller that supports Intel® DVO interface.

2.4 Miscellaneous Pins

- **HSYNC and VSYNC pins**

  HSYNC is the horizontal sync output pin. A buffered version of VGA horizontal sync can be acquired from this pin.

  VSYNC is the vertical sync output pin. A buffered version of VGA vertical sync can be acquired from this pin (See **Figure 7**). **Figure 8** shows a paradigm of VGA monitor connection in which HSYNC and VSYNC are involved.

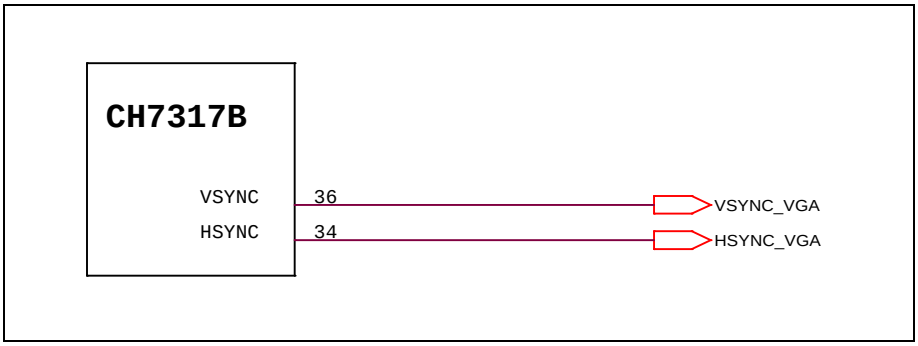


Figure 7: VSYNC and HSYNC Connection

- **BSCAN Pin**

  BSCAN pins are used for internal test purpose only. These pins can be left open.

2.5 Analog RGB Output

Table 2 shows the video out connection from the DACs of CH7317B.

Table 2: Video DAC Configuration

Output Type	DACA[0]	DACA[1]	DACA[2]
VGA	B	G	R

The R, G, B (pins 20, 24, and 28) signals are analog video signals. These signals should not be routed together. There should be a minimum of 12 mils spacing between each of the R, G, B signals and 20 mils spacing between them and any digital trace.

Typically these signals should be routed in a separate analog area without any digital signal running through the area. Corners for these traces should be at a maximum of 45 degree. 90 degree corners should not be used due to cross coupling between adjacent traces. These traces should be kept on the top layer to minimize the use of vias on them. See **Figure 8** for VGA monitor connection.

In order to minimize the hazard of ESD a set of protection diodes are recommended for all the VGA Signals including R/G/B, HSYNC/VSYNC and SD_DDC/SC_DDC.

International standard EN 55024:1998 establishes 4KV as the common immunity requirement for contact discharges in electronic systems. 8KV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

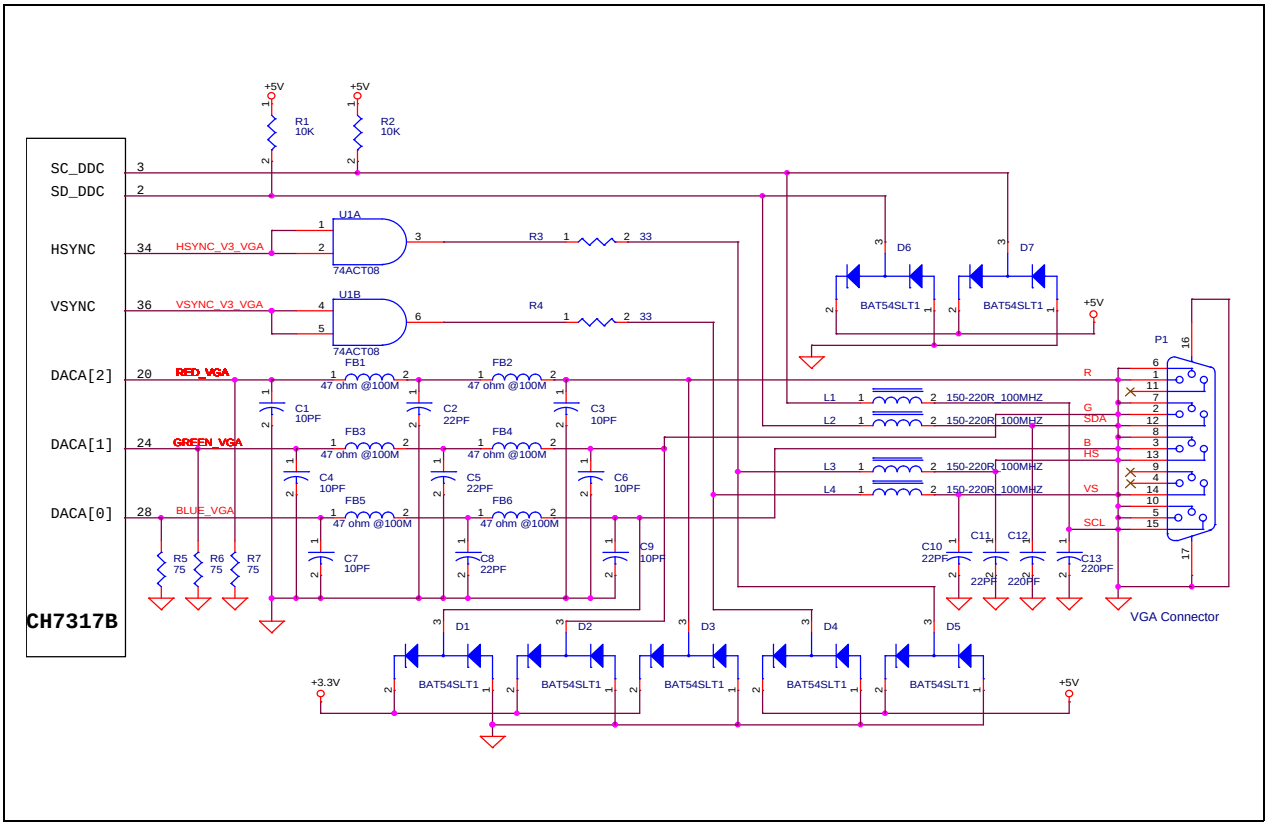


Figure 8: VGA Monitor Connection

2.6 Thermal Exposed Pad Package

The CH7317B is available in a 64 pin LQFP without thermal exposed pad and QFN with thermal exposed pad package. The part numbers are CH7317B-TEF and CH7317B-BF, respectively. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7317B.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 9**.

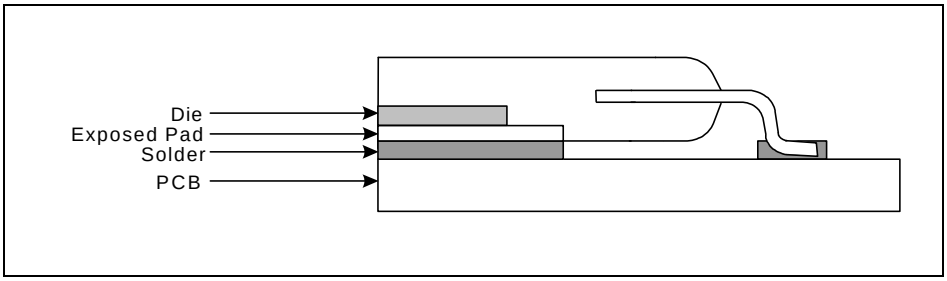


Figure 9: Cross-section of exposed pad package

We should attend the placement of the thermal land pattern. Thermal pad dimension is from 4.85mm to 6.3mm (min to max), 4.85mm x 4.85mm is the minimum size recommended for the thermal pad, and 6.3mm x 6.3mm is the maximum size. The thermal land pattern should have a 3x3 grid array of 1.5mm pitch thermal vias connected to the ground layer of the PCB. These vias should be 0.38mm in diameter with 1 oz copper via barrel plating. You can see it in **Figure 10**.

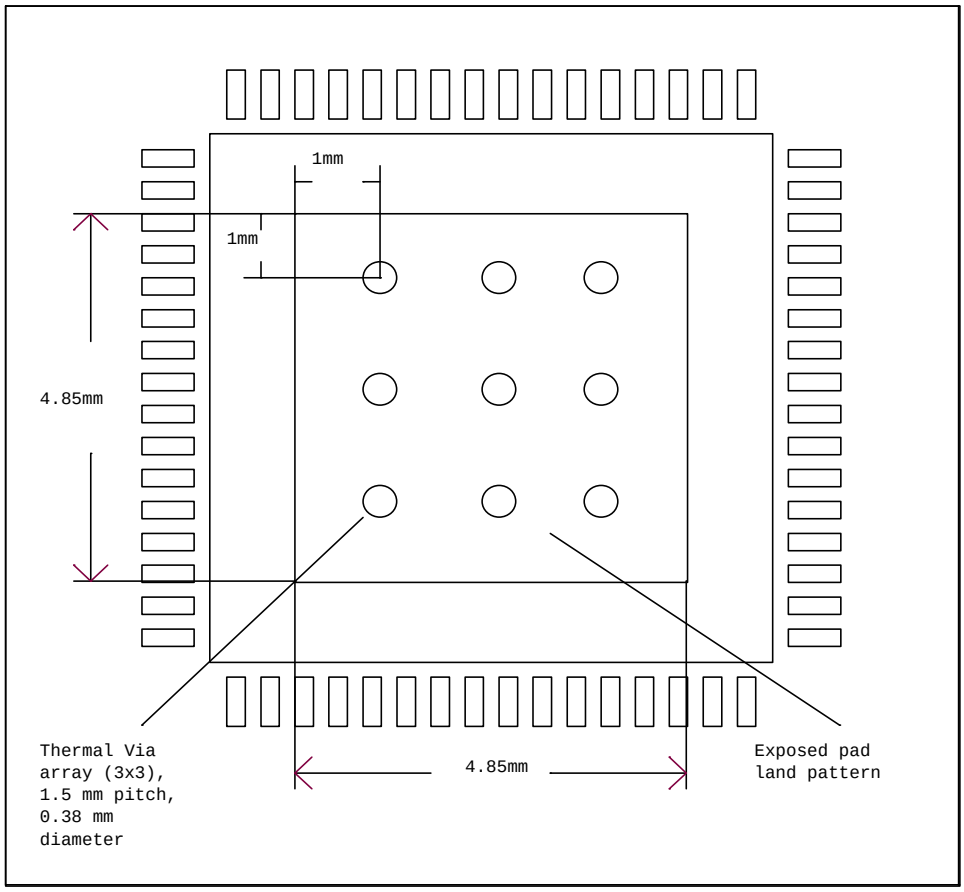


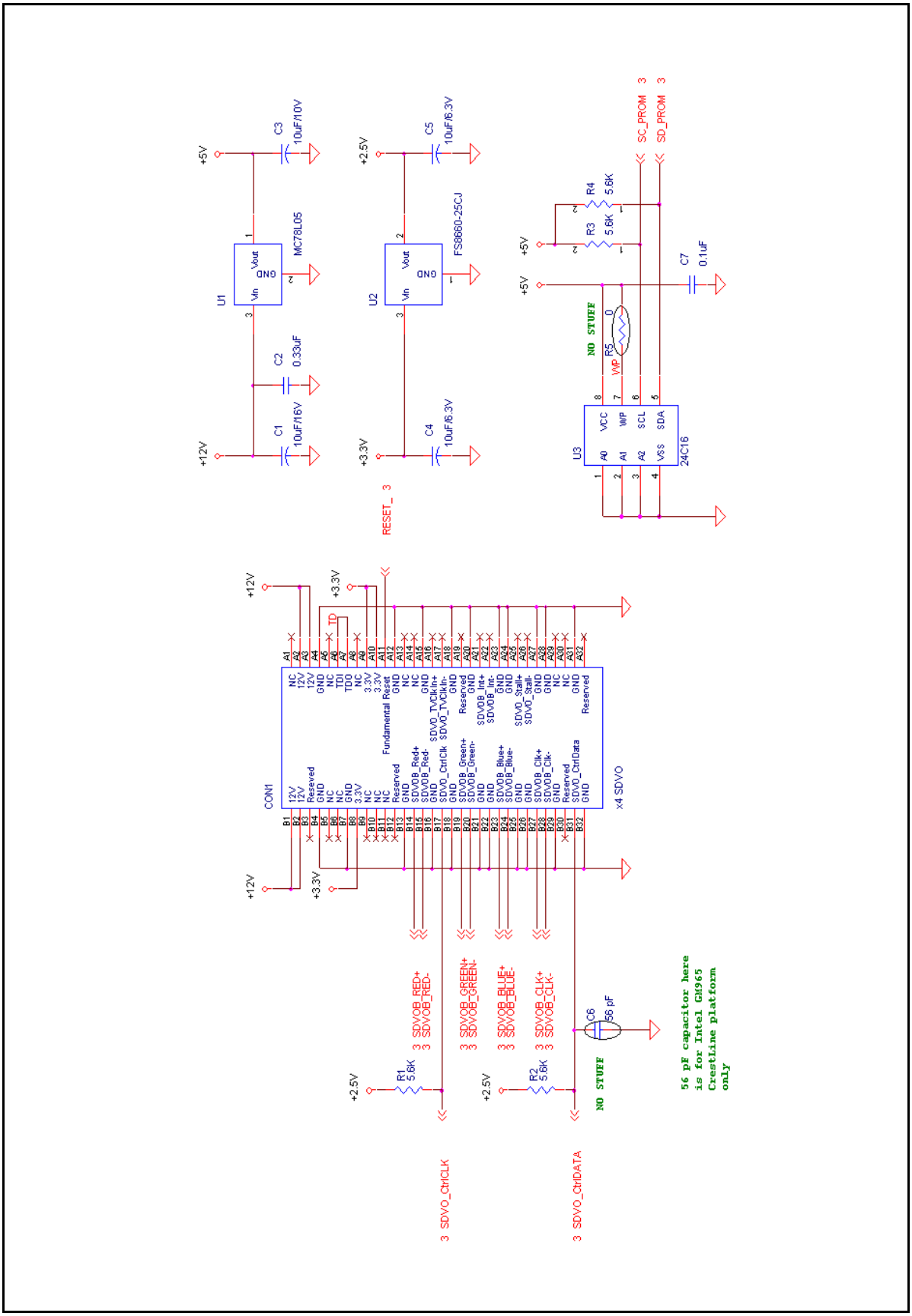
Figure 10: Thermal Land Pattern

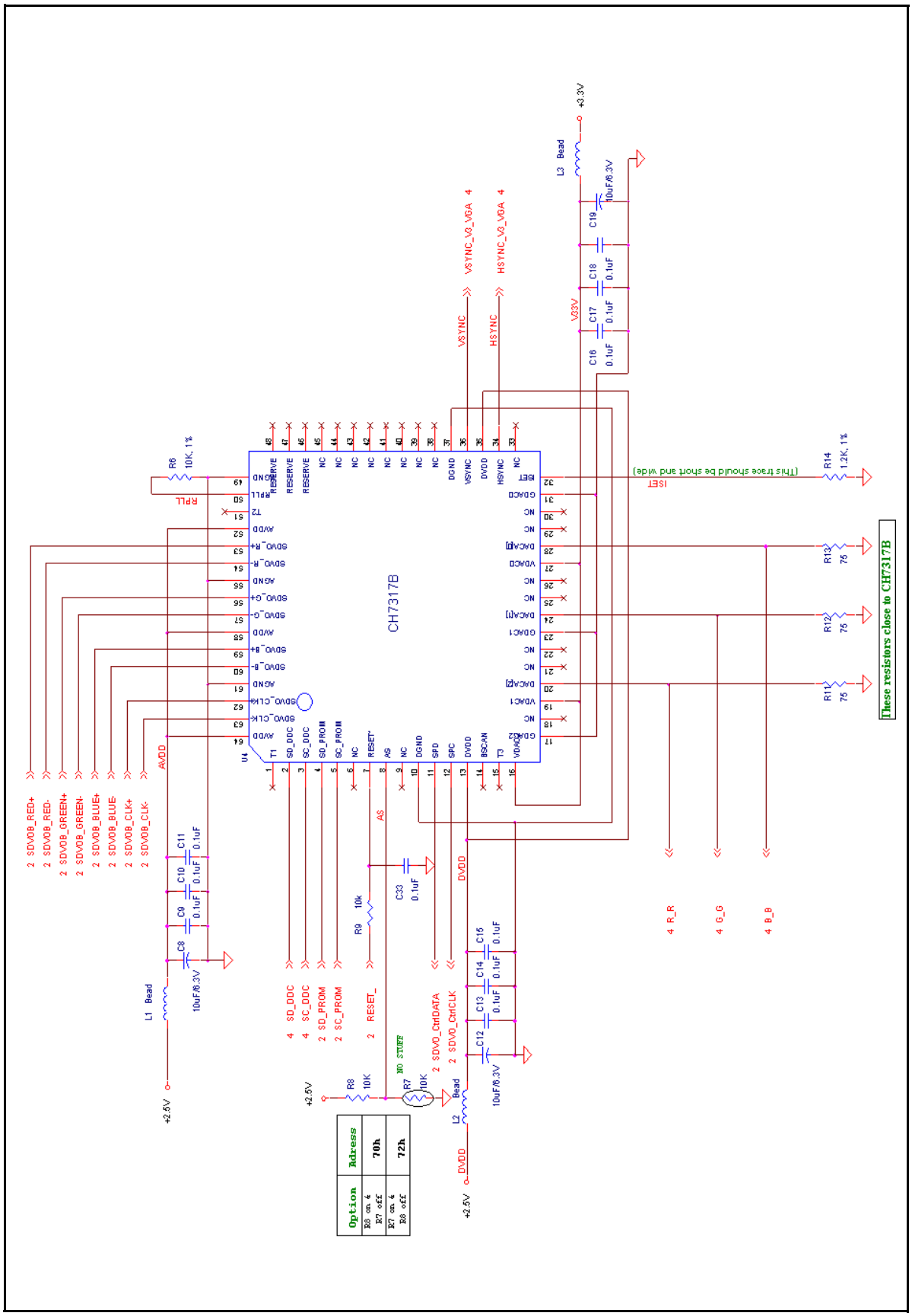
When applying solder paste to the thermal land pattern, the recommended stencil thickness is from 5 to 8 mils. Thermal resistance was calculated using the thermal simulation program called ANSYS.

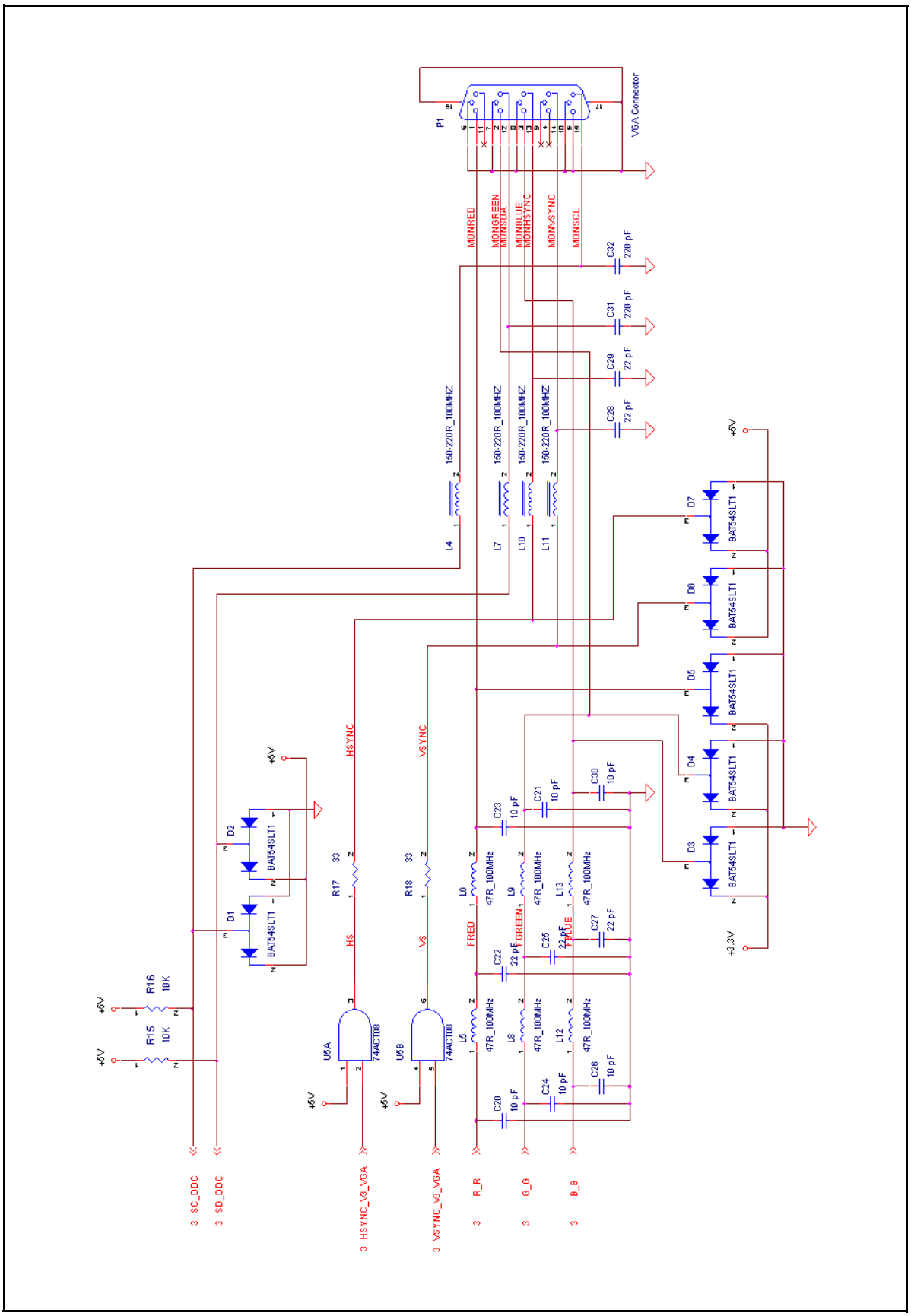
3. Reference Design Example

The following schematics are based on an Intel® Grantsdale-G graphics chipset design and are to be used as a CH7317B PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7317B and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example




CH7317B
These resistors close to CH7317B
(This trace should be short and wide)
ISET
RESET_
SD_DDC
SC_DDC
SD_PROM
SC_PROM
SDVO_CtrlDATA
SDVO_CtrlCLK
VSYNC
HSYNC
AVDD
DVDD
+2.5V
+3.3V
Option
Adress
70h
72h


P1
VGA Connector
MONRED
MONGREEN
MONSDA
MONBLUE
MONHSYNC
MONVSYNC
MONSCL
C32 220 pF
C31 220 pF
C29 22 pF
C28 22 pF
L4 150-220R_100MHZ
L7 150-220R_100MHZ
L10 150-220R_100MHZ
L11 150-220R_100MHZ
+5V
D7 BAT54SLT1
D6 BAT54SLT1
D5 BAT54SLT1
D4 BAT54SLT1
D3 BAT54SLT1
+3.3V
D2 BAT54SLT1
D1 BAT54SLT1
R16 10K
R15 10K
R17 33
R18 33
HSYNC
VSYNC
HS
VS
U5A 74ACT08
U5B 74ACT08
C23 10 pF
C21 10 pF
C30 10 pF
L6 47R_100MHz
L9 47R_100MHz
L13 47R_100MHz
FRED
FGREEN
FBLUE
C22 22 pF
C25 22 pF
C27 22 pF
L5 47R_100MHz
L8 47R_100MHz
L12 47R_100MHz
C20 10 pF
C24 10 pF
C26 10 pF
3 SC_DDC
3 SD_DDC
3 HSYNC_V3_VGA
3 VSYNC_V3_VGA
3 R_R
3 G_G
3 B_B

3.2 Evaluation Board Preliminary BOM

Item	Quantity	Reference	Part
1	1	CON1	x4 SDVO
2	1	C1	10uF/16V
3	1	C2	0.33uF
4	1	C3	10uF/10V
5	5	C4,C5,C8,C12,C19	10uF/6.3V
6	1	C6	56 pF
7	11	C7,C9,C10,C11,C13,C14,C15,C16,C17,C18,C33	0.1uF
8	6	C20,C21,C23,C24,C26,C30	10 pF
9	5	C22,C25,C27,C28,C29	22 pF
10	2	C31,C32	220 pF
11	7	D1,D2,D3,D4,D5,D6,D7	BAT54SLT1
12	3	L1,L2,L3	Bead
13	4	L4,L7,L10,L11	150-220R_100MHZ
14	6	L5,L6,L8,L9,L12,L13	47R_100MHz
15	1	P1	VGA Connector
16	4	R1,R2,R3,R4	5.6K
17	1	R5	0
18	1	R6	10K, 1%
19	5	R7,R8,R9,R15,R16	10K
20	3	R11,R12,R13	75
21	1	R14	1.2K, 1%
22	2	R17,R18	33
23	1	U1	MC78L05
24	1	U2	FS8660-25CJ
25	1	U3	24C16
26	1	U4	CH7317B
27	1	U5	74ACT08

4. Revision History

Revision	Date	Section	Description
1.0	03/13/09	All	Official release.
1.1	06/01/09	All	Add ESD information, Change CHSYNC to HSYNC.
1.2	09/18/09	All	Modify restruction filter, reference schematic, BOM.

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