CH7319 DVI Transmitter with HDCP

FEATURES

- Digital Visual Interface (DVI 1.0) Transmitter up to 165M pixels/second
- High-bandwidth Digital Content Protection (HDCP) support
- Supports switched DVI encoding two outputs port A and B one at the time
- DVI low jitter PLL
- DVI hot plug detection
- High-speed SDVO◊ (1G~2Gbps) AC-coupled serial differential RGB inputs
- Programmable power management
- Fully programmable through a serial port
- Configuration through Intel® Opcodes◊
- Windows XP and Vista support (including MCE and 64-bit variations)
- Integrated HDCP Key (HDCP 1.1)
- Offered in a 64-pin LQFP package

GENERAL DESCRIPTION

The CH7319 is a Chrontel flat panel display product targeted at PC industry. This transmitter accepts a digital RGB graphics input signal stream from the Intel's Serial Digital Video Output (SDVO) interface, performs digital processing on both data and timing and then transmits DVI signals through a DVI link.

The DVI processor includes a low jitter PLL for generation of the high frequency serialized clock, and all circuitry required to encode, serialize and transmit the data. The CH7319 is able to drive a DFP display at a pixel rate of up to 165MHz, supporting UXGA (1600x1200) resolution displays.

The CH7319 has two DVI output ports that allow two DVI monitors to be switched from a single source. Its detection circuitry will automatically route the DVI data stream to a correct DVI port that a monitor is attached to.

The CH7319 has the ability to become a HDCP rev1.1 Down-stream compliant DVI transmitter by using an internal HDCP key containing the proper device keys that can be obtained from Chrontel, Inc.

CH7319 is pin to pin compatible with CH7315 DVI/HDMI transmitter and CH7320 DVI transmitter.

◊ Intel® Proprietary.

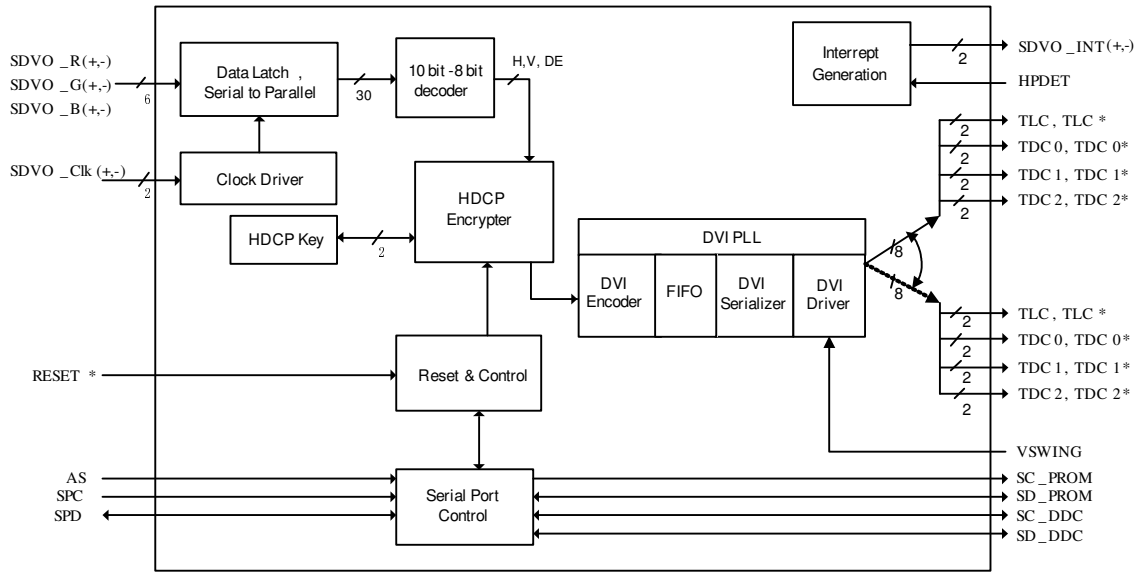

Figure 1: Functional Block Diagram

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1. PIN-OUT

1.1 Package Diagram

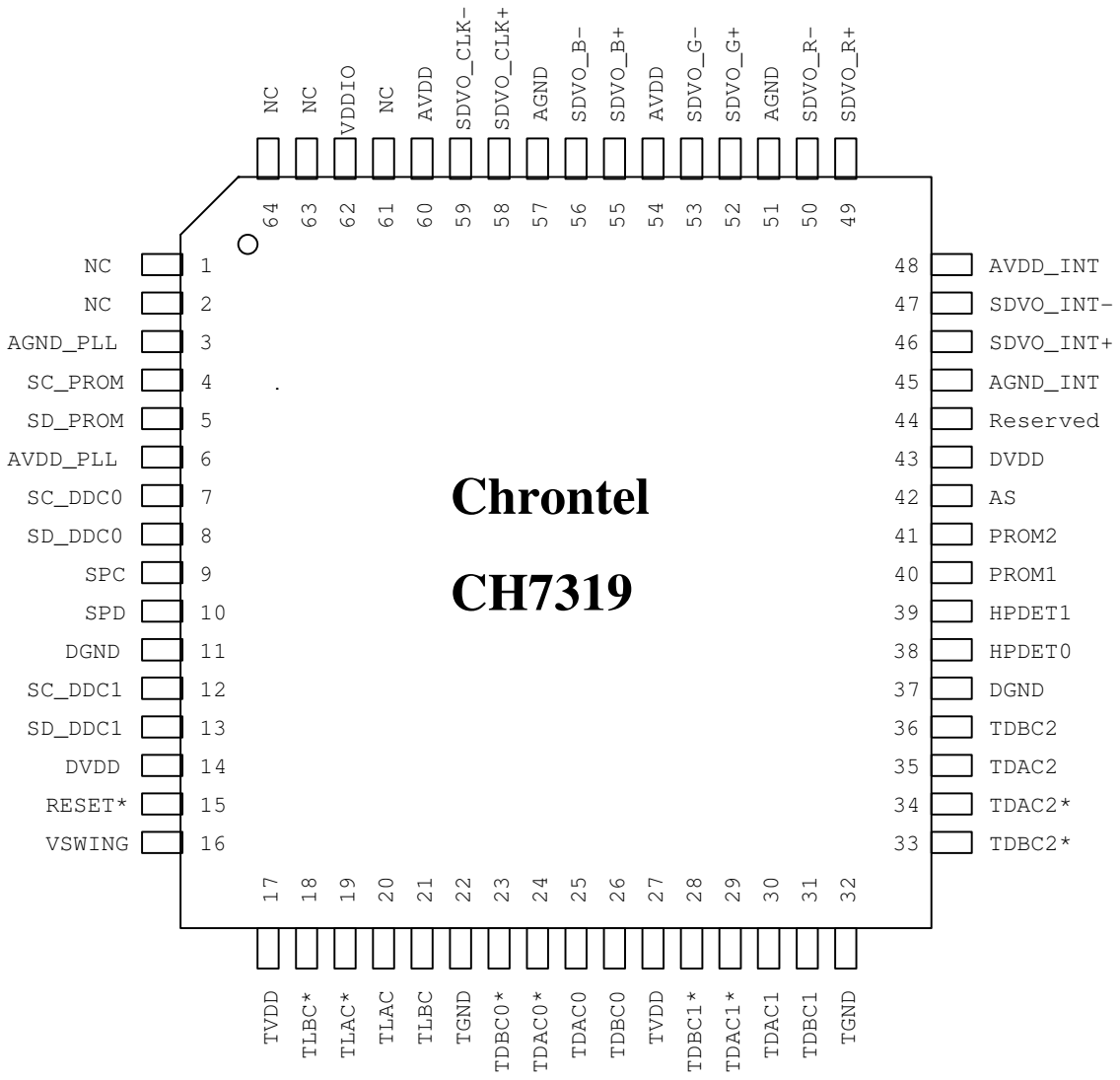

Figure 2: 64-Pin LQFP Pin Out

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1	In	Reserved	This pin must be left open (not connected) in the application.
2	In	Reserved	This pin must be left open (not connected) in the application.
4	In/Out	SC_PROM	**Routed Clock Output to PROM** This pin functions as the clock bus of the serial port to PROM on ADD2 card. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
5	In/Out	SD_PROM	**Routed Data to PROM** This pin functions as the bi-directional data pin of the serial port for PROM on ADD2 card. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
7	In/Out	SC_DDC0	**Routed Serial Port Clock to Port A DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a pull-up resistor of 1.8kΩ to the desired high state voltage. Leave open or tied high with a 10kΩ resistor if unused.
8	In/Out	SD_DDC0	**Routed Serial Port Data to Port A DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a pull-up resistor of 1.8kΩ to the desired high state voltage. Leave open or tied high with a 10kΩ resistor if unused.
9	In/Out	SPC	**Serial Port Clock Input / Output** This pin functions as the clock input of the serial port and operates with inputs from 0 to 2.5V. This pin requires an external 2.2kΩ pull up resistor to 2.5V.
10	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 2.5V. Outputs are driven from 0 to 2.5V. This pin requires an external 2.2kΩ pull up resistor to 2.5V.
12	In/Out	SC_DDC1	**Routed Serial Port Clock to Port B DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a pull-up resistor of 5.6kΩ to the desired high state voltage. This pin should be pulled low with a 10K ohm resistor (recommended) or left open if unused.
13	In/Out	SD_DDC1	**Routed Serial Port Data to Port B DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a pull-up resistor of 5.6kΩ to the desired high state voltage. This pin should be pulled low with a 10K ohm resistor (recommended) or left open if unused.
15	In	RESET*	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
16	In	VSWING	**DVI Swing Control** This pin sets the swing level of the DVI outputs. A 1.2K-ohm resistor should be connected between this pin and TGND using short and wide traces.
19, 20	Out	TLAC*, TLAC	**DVI Port A Clock Outputs** These pins provide the differential clock output for the DVI port A corresponding to data on the TDAC [2:0] outputs.
24, 25	Out	TDAC0*, TDAC0	**DVI Port A Data Channel 0 Outputs** These pins provide the DVI port A differential outputs for data channel 0 (blue).
29, 30	Out	TDAC1*, TDAC1	**DVI Port A Data Channel 1 Outputs** These pins provide the DVI port A differential outputs for data channel 1 (green).
34, 35	Out	TDAC2*, TDAC2	**DVI Port A Data Channel 2 Outputs** These pins provide the DVI port A differential outputs for data channel 2 (red).
18, 21	Out	TLBC*, TLBC	**DVI Port B Clock Outputs** These pins provide the differential clock output for the DVI port B corresponding to data on the TDBC [2:0] outputs.
23, 26	Out	TDBC0*, TDBC0	**DVI Port B Data Channel 0 Outputs** These pins provide the DVI port B differential outputs for data channel 0 (blue).

Pin #	Type	Symbol	Description
28, 31	Out	TDBC1*, TDBC1	**DVI Port B Data Channel 1 Outputs** These pins provide the DVI port B differential outputs for data channel 1 (green).
33, 36	Out	TDBC2*, TDBC2	**DVI Port B Data Channel 2 Outputs** These pins provide the DVI port B differential outputs for data channel 2 (red).
38	In	HPDET0	**Hot Plug Detect (internal pull-down)** This input pin determines whether the DVI output driver is connected to a DVI monitor. When port A is connected, the monitor is required to supply a voltage greater than 2.4 volts.
39	In	HPDET1	**Hot Plug Detect (internal pull-down)** This input pin determines whether the DVI output driver is connected to a DVI monitor. When port B is connected, the monitor is required to supply a voltage greater than 2.4 volts.
40	In/Out	PROM1	**Routed Data to PROM** This pin functions as the bi-directional data pin of the serial port for PROM on ADD2 card. This pin will require a pull-up resistor of 1.8kΩ to the desired high state voltage. Leave open if unused.
41	In/Out	PROM2	**Routed Clock to PROM** This pin functions as the clock bus of the serial port to PROM on ADD2 card. This pin will require a pull-up resistor of 1.8kΩ to the desired high state voltage. Leave open if unused.
42	In	AS	**Address Select (Internal pull-up)** This pin determines the serial port address of the device (0,1,1,1,0,0,AS*, 0). When AS is tied low (10kΩ), the address is 72h. When AS is tied high (10kΩ), the address is 70h. This pin must be externally pulled high / low.
44	In	Reserved	**Reserved (internal pull-down)** This pin must be left open (not connected) in the application.
46, 47	Out	SDVO_INT+/-	**Interrupt Output Pair associated with SDVO Data Channel** These pins output one AC-coupled differential pair of interrupt signals used as a hot plug attach/detach notification to VGA controller. Toggling between 100MHz and 200MHz on this pair is considered an assertion (‘1’ value); not toggling at all is considered a de-assertion (‘0’ value).
49, 50, 52,53, 55,56	In	SDVO_R+/-, SDVO_G+/-, SDVO_B+/-	**SDVO Data Channel Inputs** These pins accept 3 AC-coupled (100nF) differential pair of inputs from a digital video port of a graphics controller. These 3 pairs of inputs are R, G, B. The differential peak-peak input voltage has a max value of 1.2V, with a min. value of 175mV.
58,59	In	SDVO_CLK+/-	**Differential Clock Input associated with SDVO Data channel** These pins accept one AC-coupled differential pair of input from a digital video port of a graphics controller. The range of this clock pair is 100~200MHz. For specified pixel rates in specified modes this clock pair will run at an integer multiple of the pixel rate. The differential peak-peak input voltage has a max value of 1.2V, with a min. value of 175mV.
61	In	Reserved	This pin must be left open (not connected) in the application.
63	In	Reserved	This pin must be left open (not connected) in the application.
64	In	Reserved	This pin must be left open (not connected) in the application.
14,43	Power	DVDD	**Digital Supply Voltage** (2.5V)
11,37	Power	DGND	**Digital Ground**
17, 27	Power	TVDD	**DVI Transmitter Supply Voltage** (3.3V)
22,32	Power	TGND	**DVI Transmitter Ground**
45	Power	AGND_INT	**Interrupt block Ground**
48	Power	AVDD_INT	**Interrupt block Supply Voltage** (2.5V)
54, 60	Power	AVDD	**Analog Supply Voltage** (2.5V)
51, 57	Power	AGND	**Analog Ground**
3	Power	AGND_PLL	**DVI PLL Ground**
6	Power	AVDD_PLL	**DVI PLL Supply Voltage** (3.3V)
62	Power	VDDIO	**3.3V supply voltage**

2. FUNCTIONAL DESCRIPTION

2.1 Input Interface

2.1.1 Overview

One pair of differential clock signal and three differential pairs of data signals (R/G/B) form one channel data. The input data are 10-bit serialized data. Input data run at 1Gbits/s~2Gbits/s, being a 10x multiple of the clock rate (SDVO_CLK+/-). The CH7319 de-serializes the input into 10-bit parallel data with synchronization and alignment. Then the 10-bit characters are mapped into 8-bit color data or control data (HSYNC, VSYNC, DE).

2.1.2 Interface Voltage Levels

All differential SDVO pairs are AC coupled differential signals. Therefore, there is not a specified DC signal level for the signals to operate at. The differential p-p input voltage has a min of 175mV, and a max of 1.2V. The differential p-p output voltage has a min of 0.8V, with a max of 1.2V.

2.1.3 Input Clock and Data Timing

A data character is transmitted least significant bit first. The beginning of a character is noted by the falling edge of the SDVO_CLK+ edge. The skew among input lanes is required to be no larger than 2ns.

The clock rate runs at 100MHz~200MHz. The pixel rate can be 25MP/s~165MP/s. The pixel rate and the clock rate do not always equal. The clock rate can be a multiple of the pixel rate (1x, 2x or 4x depending on the pixel rate) so that the clock rate will be stay in the 100MHz~200MHz range. In the condition that the clock rate is running at a multiple of the pixel rate, there isn't enough pixel data to fill the data channels. Dummy fill characters ('0001111010') are used to stuff the data stream. The CH7319 supports the following clock rate multipliers and fill patterns shown in Table 2.

Table 2: CH7319 supported Pixel Rates, Clock Rates, Data Transfer Rates and Fill Patterns

Pixel Rate	Clock Rate – Multiplier	Stuffing Format	Data Transfer Rate - Multiplier
25~50 MP/s	100~200 MHz – 4xPixel Rate	Data, Fill, Fill, Fill	1.00~2.00Gbits/s – 10xClock Rate
50~100 MP/s	100~200 MHz – 2xPixel Rate	Data, Fill	1.00~2.00Gbits/s – 10xClock Rate
100~200 MP/s	100~200 MHz – 1xPixel Rate	Data	1.00~2.00Gbits/s – 10xClock Rate

2.1.4 Synchronization

Synchronization and channel-to-channel de-skewing is facilitated by the transmission of special characters during the blank period. The CH7319 synchronizes during the initialization period and subsequently uses the blank periods to re-synch to the data stream.

2.2 DVI Transmitter

2.2.1 DVI Output Timing

Serialized input data, sync and clock signals are input to the CH7319 from the graphics controller's digital output port. Input is through three differential data pairs and one differential clock pair. The data rate is in the range of 1.0~2.0Gbits/s. The clock rate, independent with pixel rate, is 1/10 of the data rate, resulting in the range of 100M~200MHz. Horizontal sync and vertical sync information are embedded in the data stream. Some examples of modes supported are shown in the Table 3. For Table 3, input pixel frequencies for given modes were taken from VESA DISPLAY MONITOR TIMING SPECIFICATIONS if they were detailed there, not VESA TIMING DEFINITION FOR FLAT PANEL MONITORS. The device is not dependent upon this set of timing specifications. Any values of input pixels/line, lines/frame and clock rate are acceptable, as long as the pixel rate remains below 165MHz.

Table 3: DVI Output Formats

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	Refresh Rate (Hz)	Input pixel Frequency (MHz)	DVI Frequency (Mbits/Sec)
720x400	4:3	1.35:1.00	<85	<35.5	<355
640x400	8:5	1:1	<85	<31.5	<315
640x480	4:3	1:1	<85	<36	<360
800x600	4:3	1:1	<85	<57	<570
1024x768	4:3	1:1	<85	<95	<950
1280x720	16:9	1:1	<85	<110	<1100
1280x768	15:9	1:1	<85	<119	<1190
1280x1024	4:3	1:1	<85	<158	<1580
1366x768	16:9	1:1	<85	<140	<1400
1360x1024	4:3	1:1	<75	<145	<1450
1400x1050	4:3	1:1	<75	<156	<1560
1600x1200	4:3	1:1	<60	<165	<1650

Table 4: Popular Panel Sizes

UXGA	1600x1200
SXGA+	1400x1050
	1360x1024
SXGA	1280x1024
	1280x960
XGA	1024x768
	1024x600
SVGA	800x600

2.2.2 DVI Output Ports Switch

The CH7319 has a build-in switch allows two DVI monitors to be switched from a single link DVI video source. The auto-detection mechanism inside of CH7319 will automatically sense the connection from either of the DVI ports, and switch to the correct port; allowing for a seamless and user friendly switching. Please see Figure 1.

2.3 HDCP Compatibility

High Bandwidth Digital Content Protection (HDCP) provides a means of protecting the video transmission between a DVI video transmitter and a DVI video receiver. The content protection system includes a process of (a) authentication in which the video transmitter verifies that a given video receiver is licensed to receive protected content; (b) encryption in which the transmitted video data is encrypted based on secret codes exchanged during the authentication process; and (c) renewability in which the video transmitter can identify compromised receivers and prevent the transmission of protected content.

Each HDCP authorized device (transmitter or receiver) has an array of 40, 56-bit secret device keys and a Key Selection Vector (KSV) obtainable from Digital Content Protection LLC (http://www.digital-cp.com/). With the addition of the encrypted HDCP device keys, the CH7319 can be configured to be a HDCP compliant transmitter. A possible connection diagram is shown in the following figure.

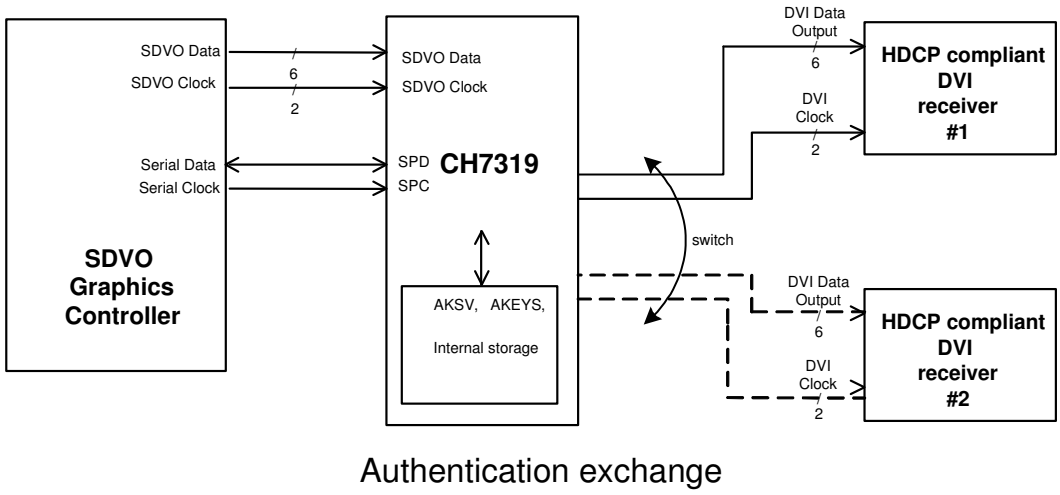

Figure 3: **Possible Connection Diagram for HDCP**

When the CH7319 is configured as an HDCP non-compliant device, it will not send necessary information to the graphics controller to be identified as an HDCP compliant device. As a result, the graphics controller will not send any data that require content protection. Also, the HDCP process is bypassed inside the CH7319.

Details of the CH7319 HDCP operation are available in a separate document. Contact Chrontel for details. See also the "High Bandwidth Digital Content Protection System" specification available at http://www.digital-cp.com/.

2.4 Command Interface

Communication is through two-wire path, control clock (SPC) and data (SPD). The CH7319 accepts incoming control clock and data from graphics controller, and is capable of redirecting that stream to an ADD2 card PROM, DDC, or CH7319 internal registers. The control bus is able to run up to 1MHz when communicating with internal registers, up to 400kHz for the PROM and up to 100kHz for the DDC.

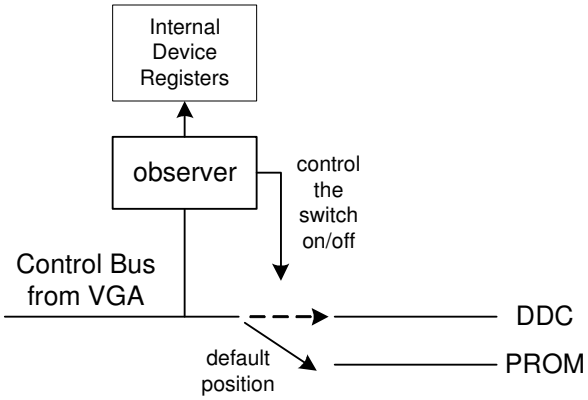

Figure 4: Control Bus Switch

Upon reset, the default state of the directional switch is to redirect the control bus to the ADD2 PROM. At this stage, the CH7319 observes the control bus traffic. If the observing logic sees a control bus transaction destined for the internal registers (device address 70h or 72h), it disables the PROM output pairs, and switches to internal registers. In the condition that traffic is to the internal registers, an opcode command is used to set the redirection circuitry to the appropriate destination (ADD2 PROM or DDC). Redirecting the traffic to internal registers while at the stage of traffic to DDC occurs on observing a STOP after a START on the control bus.

3. REGISTER CONTROL

The CH7319 is controlled via a serial control port. The serial bus uses only the SC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device will retain all register values during power down modes.

Registers 00h to 11h are reserved for opcode use. All registers except bytes 00h to 11h are reserved for internal factory use. For details regarding Intel® SDVO opcodes, please contact Intel®.

4. ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

Table 5: T_{SC}, T_{AMB}, T_{STOR}, T_J, T_{VPS} Ratings

Symbol	Description	Min	Typ	Max	Units
	All 2.5V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		3.5 5.0	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 second)			260	°C
	Vapor phase soldering (11 second)			245	
	Vapor phase soldering (60 second)			225	

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can cause permanent damage.

4.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Analog Power Supply Voltage	2.375	2.5	2.625	V
AVDD_INT	Analog interrupt Power Supply Voltage	2.375	2.5	2.625	V
AVDD_PLL	Analog PLL Power Supply Voltage	3.100	3.3	3.500	V
DVDD	Digital Power Supply Voltage	2.375	2.5	2.625	V
TVDD	DVI Power Supply	3.100	3.3	3.500	V
VDDIO	Misc. Power Supply voltage	1.425		3.500	V
VDD33	Generic for all 3.3V supplies	3.100	3.3	3.500	V
VDD25	Generic for all 2.5V supplies	2.375	2.5	2.625	V
T_{AMB}	Ambient operating temperature (Commercial / Automotive Grade 4)	0		70	°C
T_{AMB}	Ambient operating temperature (Industrial / Automotive Grade 3)	-40		85	°C

4.3 Electrical Characteristics

(Operating Conditions: T_A = 0°C to 70°C for parts qualified as Commercial / Automotive Grade 4, T_A = –40°C to 85°C for parts qualified as Industrial / Automotive Grade 3, VDD25 =2.5V ± 5%, VDD33=3.3V± 5%)

Table 7: Electrical Characteristics

Symbol	Description	Min	Typ	Max	Units
I_{VDD25}	Total VDD25 supply current (2.5V supplies) Pixel Rate=162MHz		210		mA
I_{VDD33}	Total VDD33 supply current (3.3V supply) Pixel Rate=162MHz		75		mA
I_{PD}	Total Power Down Current (all supplies)		100		uA

4.4 DC Specifications

Table 8: DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$V_{RX\text{-}DIFFp\text{-}p}$	SDVO Receiver Differential Input Peak to Peak Voltage	$V_{RX\text{-}DIFFp\text{-}p} = 2 * \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$	0.175		1.200	V
$Z_{RX\text{-}DIFF\text{-}DC}$	SDVO Receiver DC Differential Input Impedance		80	100	120	Ω
$Z_{RX\text{-}COM\text{-}DC}$	SDVO Receiver DC Common Mode Input Impedance		40	50	60	Ω
$Z_{RX\text{-}COM\text{-}INITIAL\text{-}DC}$	SDVO Receiver Initial DC Common Mode Input Impedance	Impedance allowed when receiver terminations are first turned on	5	50	60	Ω
$V_{INT\text{-}DIFFp\text{-}p}$	SDVO INT Differential Output Peak to Peak Voltage		0.8		1.2	V
V_{SPOL} [1]	Serial Port Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH} [2]	Serial Port Input High Voltage		2.0		VDD25 + 0.5	V
V_{SPIL} [2]	Serial Port Input Low Voltage		GND-0.5		0.4	V
V_{HYS} [2]	Serial Port Input Hysteresis		0.25			V
V_{DDCIH}	DDC Serial Port Input High Voltage		4.0		VDD5 + 0.5	
V_{DDCIL}	DDC Serial Port Input Low Voltage		GND-0.5		0.4	V
V_{PROMIH}	PROM Serial Port Input High Voltage		4.0		VDD5 + 0.5	
V_{PROMIL}	PROM Serial Port Input Low Voltage		GND-0.5		0.4	V

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SD_DDCOL}[3]	SPD (serial port data) Output Low Voltage from SD_DDC (or SD_PROM)	Input is V_{INL} at SD_DDC or SD_PROM. 2.2kΩ pull-up to 2.5V.			$0.9*V_{INL} + 0.25$	V
V_{DDCOL}[4]	SC_DDC and SD_DDC Output Low Voltage	Input is V_{INL} at SPC and SPD. 1.8kΩ pull-up to 5.0V.			$0.933*V_{INL} + 0.35$	V
V_{PROMOL}[5]	SC_PROM and SD_PROM Output Low Voltage	Input is V_{INL} at SPC and SPD. 5.6kΩ pull-up to 2.5V.			$0.933*V_{INL} + 0.35$	V
$V_{MISC1IH}$[6]	RESET* Input High Voltage		2.7		VDD33 + 0.5	V
$V_{MISC1IL}$[6]	RESET* Input Low Voltage		GND-0.5		0.5	V
$V_{MISC2IH}$[7]	AS Input High Voltage		2.0		VDD25 + 0.5	V
$V_{MISC2IL}$[7]	AS Input Low Voltage	DVDD=2.5V	GND-0.5		0.5	V
$V_{MISC3IH}$	HPDET0, HPDET1, Input High Voltage		1.4		3.72	V
$V_{MISC3IL}$	HPDET0, HPDET1, Input Low Voltage		GND-0.5		0.5	V
$I_{MISC1PU}$	RESET* Pull Up Current	V_{IN} = 0V	10		40	uA
$I_{MISC2PD}$	HPDET0, HPDET1 Pull Down Current	V_{IN} = 2.5V V_{IN} = 2.5V	5 10		20 40	uA uA
$I_{MISC2PU}$	AS Pull Up Current	V_{IN} = 0V	10		40	uA
V_H	DVI Single Ended Output High Voltage	TVDD = 3.3V ± 5% R_{TERM} = 50Ω ± 1% R_{SWING} = 1200Ω ± 1%	TVDD – 0.01		TVDD + 0.01	V
V_L	DVI Single Ended Output Low Voltage		TVDD – 0.6		TVDD – 0.4	V
V_{SWING}	DVI Single Ended Output Swing Voltage		400		600	mVp-p
V_{OFF}	DVI Single Ended Standby(off) Output Voltage		TVDD – 0.01		TVDD + 0.01	V
I_{OFF}	DVI Single Ended Standby(off) Output Current				10	uA

Notes:

1. Refers to SPD. V_{SPOL} is the output low voltage from SPD when transmitting from internal registers not from DDC, EPROM or system.
2. Refers to SPC and SPD.
3. V_{SD_DDCOL} is the output low voltage at the SPD pin when the voltage at SD_DDC or SD_PROM is V_{INL}. Maximum output voltage has been calculated with the worst case of pull-up of 2.2kΩ to 2.5V on SPD. There are two DDC SPP interface, SC_DDC0/1 and SD_DDC0/1.
4. V_{DDCOL} is the output low voltage at the SC_DDC and SD_DDC pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 1.8k pull-up to 5V on SC_DDC and SD_DDC.
5. V_{PROMOL} is the output low voltage at the SC_PROM and SD_PROM pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 5.6kΩ pull-up to 2.5V on SC_PROM and SD_PROM.
6. V_{MISC1} refers to RESET* input which is 3.3V compliant.
7. V_{MISC2} refers to AS, HPDET0, and HPDET1. AS is 2.5V compliant. HPDET0/1 can compliant with 4.5V

4.5 AC Specifications

Table 9: AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
UI_{DATA}	SDVO Receiver Unit Interval for Data Channels		Typ. – 300ppm	1/[Data Transfer Rate]	Typ. + 300ppm	ps
f_{SDVO_CLK}	SDVO CLK Input Frequency		100		200	MHz
f_{PIXEL}	DVI Transmitter Pixel Rate		25		165	MHz
f_{SYMBOL}	SDVO Receiver Symbol Frequency		1		2	GHz
t_{RX-EYE}	SDVO Receiver Minimum Eye Width		0.4			UI
$t_{RX-EYE-JITTER}$	SDVO Receiver maximum time between jitter median and maximum deviation from median				0.3	UI
$V_{RX-CM-Acp}$	SDVO Receiver AC Peak Common Mode Input Voltage				150	mV
$RL_{RX-DIFF}$	Differential Return Loss	50MHz – 1.25GHz	15			dB
RL_{RX-CM}	Common Mode Return Loss	50MHz – 1.25GHz	6			dB
t_{SKEW}	SDVO Receiver Total Lane to Lane Skew of Inputs	Across all lanes			2	ns
T_{DVIR}	DVI Output Rise Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
T_{DVIF}	DVI Output Fall Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{SKDIFF}	DVI Output intra-pair skew	f_{XCLK} = 165MHz			90	ps
t_{SKCC}	DVI Output inter-pair skew	f_{XCLK} = 165MHz			1.2	ns
T_{DVIJIT}	DVII Output Clock Jitter	f_{XCLK} = 165MHz			150	ps

5. PACKAGE DIMENSIONS

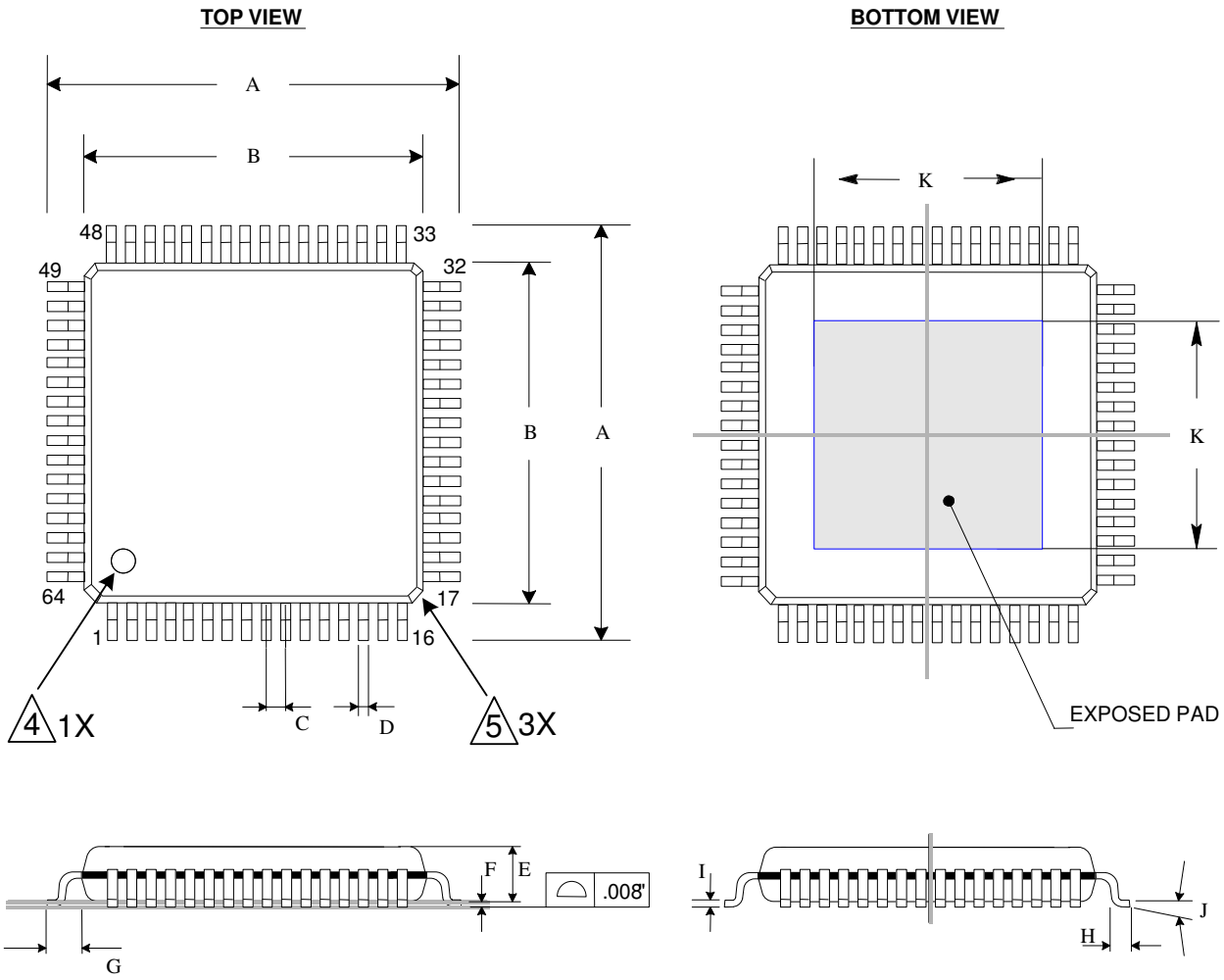

Figure 5: 64 Pin LQFP (Exposed Pad) Package

Table of Dimensions

No. of Leads		SYMBOL										
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°	5.85
	MAX				0.27	1.45	0.15		0.75	0.20	7°	7

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.
4. (1X) Corner in quadrant with Pin1 identifier (dot) is always chamfered. Exact shape of chamfer is optional.
5. (3X) Corners in quadrants without Pin1 identifier (dot) may be square or chamfered. Exact shape of corner or chamfer is optional.

6. REVISION HISTORY

Table 10: Revisions

Rev. #	Date	Section	Description
1.0	3/26/2007	All	Initial release.
1.1	8/13/2007	Ordering Information	Updated Chrontel part number.
1.2	9/7/2007	1.2 & 4.4	Updated Pin 9, Pin 10, Pin 12 and Pin 13 in Table 1& Table 9.
1.3	12/7/2007	4.2 & 4.4	Updated 4.2 Table 6 and 4.4 Table 8.
1.4	1/27/2009	4.1, 4.2, 4.3 5.0	Update the temperature range. Update 5.0 Package Dimensions and Chrontel part number.
1.5	4/6/2011	4.1, 4.2	Update operating temperatures.
1.6	6/15/2012	1.1, 1.2, 4.1, 4.2, 4.3, 5	Update ambient operating temperature into Commercial / Automotive Grade 4 and Industrial / Automotive Grade 3. Modify the description of pin 12 and pin 42 and some "Absolute Maximum Ratings". Modify "package Diagram". Add some notes for "Package Dimensions".
1.7	1/7/2014	1.2, 4.1, 4.2	Pins 46/47 (SDVO_INT+/-) and 58/59 (SDVO_CLK+/-) should be AC-coupled. Move T_{AMB} from 4.1 to 4.2.

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ORDERING INFORMATION

Part Number	Package Type	Number of Pins	Voltage Supply	Temperature Grade
CH7319A-TEF	Lead Free LQFP with exposed pad	64	2.5V & 3.3V	Commercial / Automotive Grade 4
CH7319A -TEF-I	Lead Free LQFP with exposed pad	64	2.5V & 3.3V	Industrial / Automotive Grade 3
CH7319A -TEF-TR	Lead Free LQFP with exposed pad in Tape & Reel	64	2.5V & 3.3V	Commercial / Automotive Grade 4
CH7319A -TEF-I-TR	Lead Free LQFP with exposed pad in Tape & Reel	64	2.5V & 3.3V	Industrial / Automotive Grade 3

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