PCB Layout and Design Guide for CH7511B and CH7512B

1.0 INTRODUCTION

Chrontel's CH7511B/7512B is an eDP/DP receiver that integrates LVDS Transmitter for the notebook/AIO display. The CH7511B is designed to comply with the Embedded Display Port Specification 1.2 and the CH7512B is designed to comply with the Display Port Specification 1.1a. The CH7511B/7512B provides support for two main link lanes with data rate running at either 1.62Gb/s or 2.7Gb/s, and accepts data in 18-bit 6:6:6 or 24-bit 8:8:8 RGB digital format. During system power-up, setting the power on/off sequence for a particular panel can be achieved through the CH9904 Boot ROM registers. The CH7511B/7512B has incorporated a brightness control function to interface with LCD backlight module. Brightness control commands sent through AUX Channel are dynamically translated by the CH7511B/7512B and converted into the LCD backlight control signals.

The CH7511B/7512B can support 18-bit Single Port, 18-bit Dual Port, 24-bit Single Port and 24-bit Dual Port LVDS outputs in both OpenLDI and SPWG bit mapping for LVDS application. The CH7511B/7512B supports LVDS output up to 1920x1200.

This application note focuses only on the basic PCB layout and design guidelines for the CH7511B/7512B eDP/DP Receiver with LVDS Transmitter. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures presented in this document are based on the 68-pin QFN (8x8 mm) package of the CH7511B/7512B. Please refer to the CH7511B/7512B datasheet for details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7511B/7512B should be placed as close as possible to the respective pins. The following will describe guidelines on how to connect critical pins, as well as the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimal power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor at each of the power supply pins as shown in Figure 1. These capacitors (C1, C2, C3, C4, C5, C7, C8, C10, C11, and C12) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7511B/7512B ground pins, in addition to ground vias.

2.1.1 Ground Pins

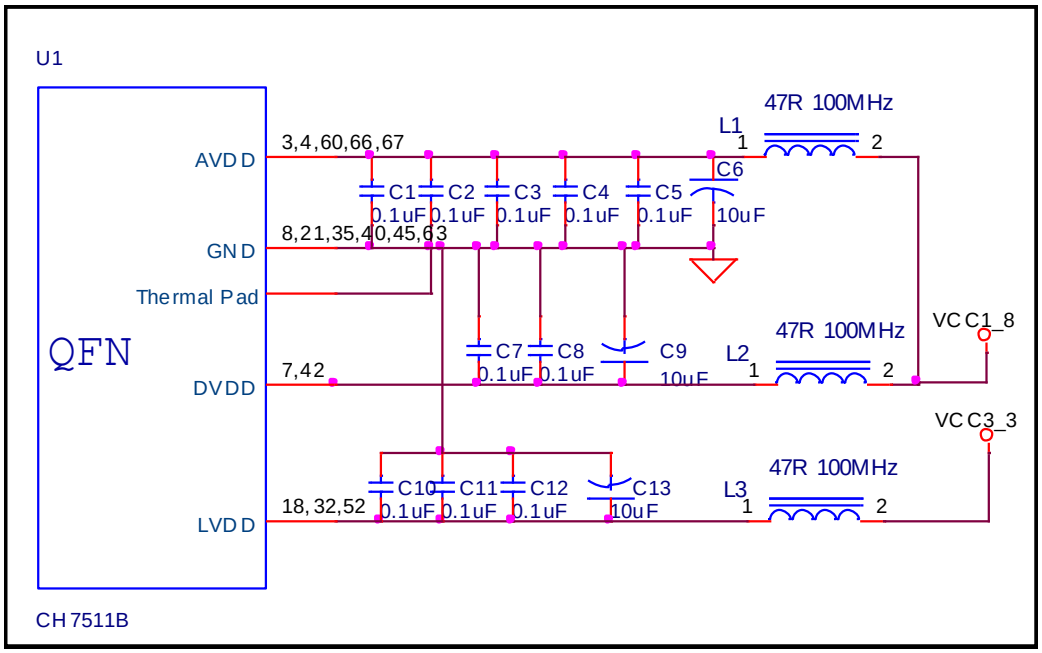
The CH7511B/7512B should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7511B/7512B ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to Table 1 for the Ground pin assignments.

2.1.2 Power Supply Pins

There are eleven power supply pins: AVDD, DVDD, LVDD, and VDDGPO. Refer to Table 1 for the Power supply pin assignments. Refer to Figure 1 for Power Supply Decoupling.

Table 1: Power Supply Pin Assignments for the CH7511B/7512B (68QFN)

Pin	# of Pins	Type	Symbol	Description
7,42	2	Power	DVDD	Digital supply voltage (1.8V)
3,4,60,66,67	5	Power	AVDD	Analog supply voltage (1.8V)
18,32,52	3	Power	LVDD	LVDS driver supply voltage and GPIO supply voltage (3.3V)
8,21,35,40,45,63, Thermal pad	6	Ground	GND	Power ground



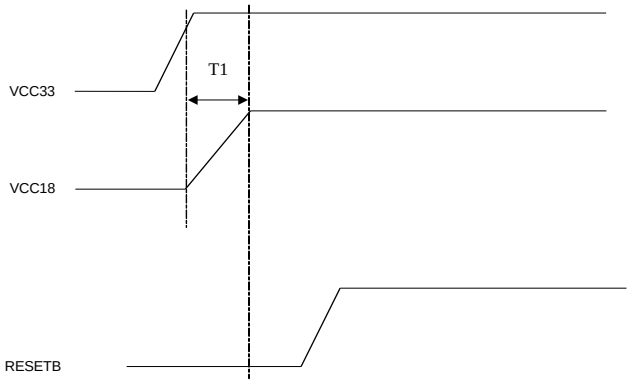


Figure 1: Power Supply Decoupling and Distribution

Note:

1. **Pease make sure that the voltage of LVDD (VCC33) should be supplied before the voltage of DVDD and AVDD (VCC18).**
2. **The RESETB signal should be supplied to the CH7511B/7512B after the powers are stable.**
3. **T1 (the VCC18 rise slope time) should not be larger than 2ms.**
4. **The exposed pad, which is the thermal pad, must be linked to GND.**
5. **All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ωat 100MHz. Refer to Fair Rite part #2743019447 for details (an equivalent part can be used for the diagram).**

2.2 Internal Reference Pins

• RBIAS pin

This pin sets the Band-gap Bias Voltage. A 10 KΩ, 1% tolerance resistor should be connected between RBIAS and GND as shown in Figure 2. A smaller resistance will create less Band-gap Bias voltage. The distance between the resistor and the CH7511B/CH7512B should be less than 6mm, the shorter and wider trace the better. For optimal performance, this signal should not overlay the analog power or analog output signals.

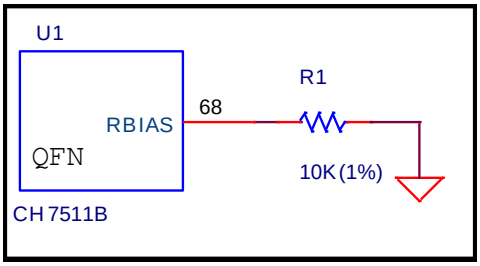


Figure 2: RBIAS Pin Connection

2.3 General Control Pins

• RESETB

This pin is the chip reset pin for the CH7511B/7512B. The RESETB pin is internally pulled-up. But when it is pulled-low, this pin places the device in the power-on-reset condition. As shown in Figure 3, one 10KΩ resistor is necessary to be pulled high to DVDD (1.8V). One 0.1uf capacitor is recommended to be pulled low to GND. After the powers are stable, send the RESETB signal (low to high) to the chip, as shown in Figure 1.

- Option1: link the RESETB signal to the external GPIO_PCH signal (1.8V).
- Option2: add the level shifter circuits to link the RESETB signal to the GPIO_PCH signal (3.3V).

• XI, XO

A 27MHz crystal (±30ppm) can be connected to XI and XO as the CH7511B/7512B the optional reference clock input. In PCB design, a 27MHz crystal must be placed as close as possible to the XI and XO pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates the timing reference for the CH7511B/7512B, it is essential that noise not couple into these input pins.

The crystal load capacitance, CL, is usually specified in the crystal spec from the vendor. Refer to Figure 3 for a crystal circuit reference design and an example of load capacitors.

• REFCK

The REFCK is another optional pin as the reference input clock for the CH7511B/7512B. A 27MHz (3.3V) clock may be injected at this pin as shown in Figure 3. For PCB design, the capacitor must be placed as close as possible to the REFCK pin, with traces connected from point to point, overlaying the ground plane.

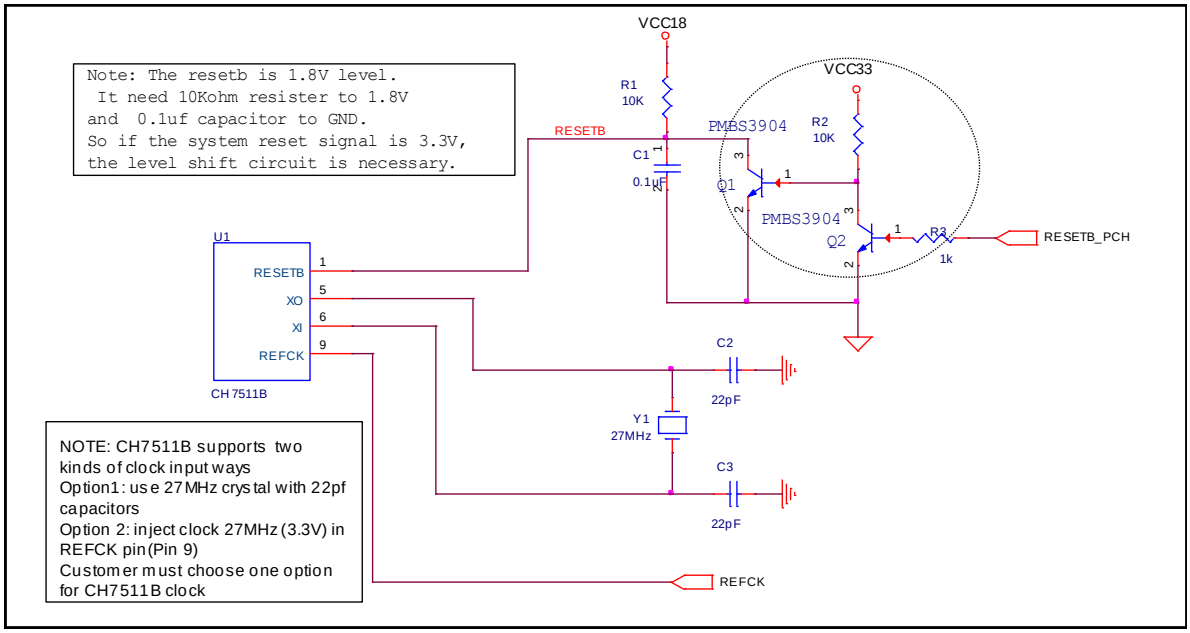


Figure 3: General Control Pins

2.4 Serial Port Control Pins

• SPC0 and SPD0

SPD0 and SPC0 function as a serial interface where SPD0 is the bi-directional data and SPC0 is an input-only serial clock. In the reference design, SPD0 and SPC0 pins are pulled up to LVDD (+3.3V) with 6.8k resistors. Through these two pins, the internal register values of the chip can be read. The external Boot ROM can be updated if these pins are connected to SPC1 and SPD1 with jumpers as shown in Figure 4.

• SPC1 and SPD1

SPD1 and SPC1 function as a serial interface where SPD1 is bi-directional data and SPC1 is an input only serial clock. In the reference design, SPD1 and SPC1 pins are pulled up to LVDD (+3.3V) with 6.8kΩ resistors as shown in Figure 4.

SPD1 and SPC1 are used to interface with the CH9904 (the serial Boot ROM). The CH7511B/7512B will auto-load the values, such as EDIDs and configurations, etc., from the Boot ROM upon power-on or reset.

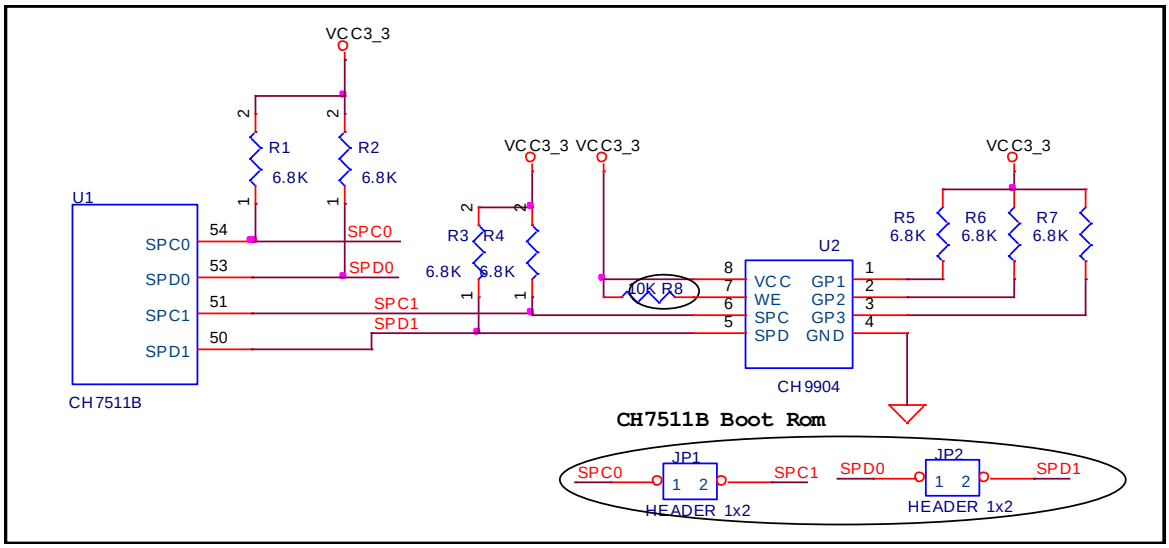


Figure 4: Serial Port Control

Note:

If you use SPC0/SPD0 or the AUX channel to update the CH9904 Boot ROM, the precondition is that the MCU firmware must work properly. It is recommended that the IIC/SMBUS be used to update CH9904, by linking the IIC/SMBUS to SPC0 and SPD0

2.5 Display Port Signal Pins

• DP0P/N, DP1P/N

These pins accept two AC-coupled differential pair signals from the Display Port transmitter.
Since the digital serial data of the CH7511B/7512B may be toggled at speeds up to 2.7 GHz, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7511B/7512B be kept as short as possible, avoid discontinuities in the reference plane and be isolated as much as possible from the analog outputs and analog circuitry. For optimal performance, these signals should not overlay the analog power or analog output signals. When a signal pair has to changes layers, the ground stitching vias should be placed close to the signal vias. A minimum of 1 to 3 stitching vias per pair of signals is recommended. Never route a trace so that it straddles a plane split. It is recommended that 5 mils traces be used in routing these signals. There should be 7 mils spacing between each intra pair. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches. Bend smaller than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH, as shown in Figure 5.

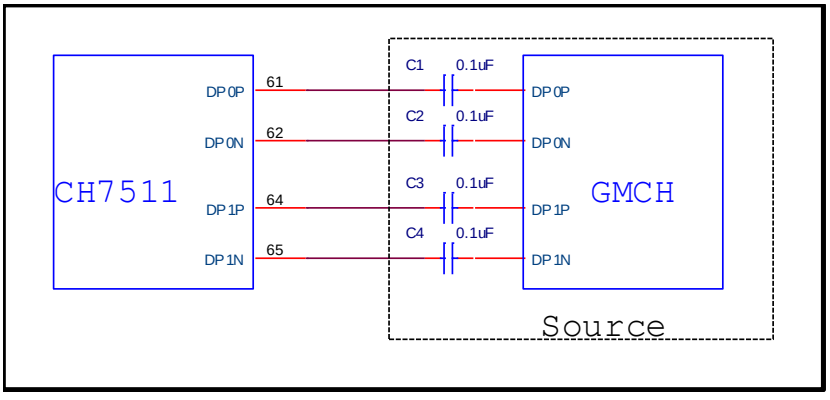


Figure 5: CH7511B/7512B DP Main Link Lane Inputs

• AUXP and AUXN

These two pins are for Display Port AUX channel control that accepts a half-duplex, bi-directional AC-coupled differential signal. An AC coupling capacitor, 0.1uF recommended, must be placed on the end as shown in Figure 6.

• HPDET

This output pin indicates whether the device is active or not. It also generates an interrupt pulse as defined by the Display Port standard. Output voltage is 3.3V. A resistor, greater than 100KΩ, should be connected between this pin and GND as shown in Figure 6.

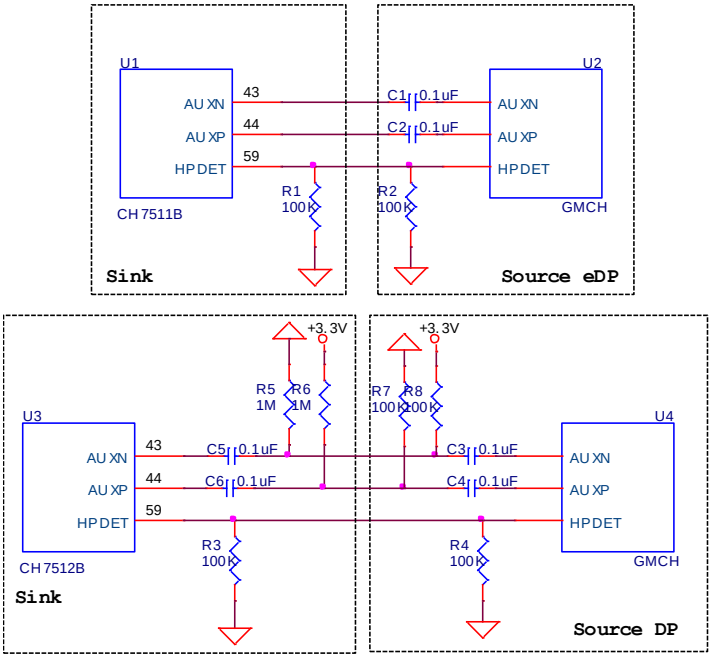


Figure 6: CH7511B/7512B AUX channel and HPDET

2.6 LVDS Signal Pins

• LVDS Outputs (LDCxP and LDCxN)

The LVDS output signals are LDCxP and LDCxN. The LVDS is a differential interface with a nominal swing 200mV. The following rules should be applied to the signals:

1. Keep traces as short as possible.
2. Make these traces have 100Ω differential impedance.
3. Trace widths should be 5 mils.
4. Intra Pair spacing (spacing between the "+" and "-" pairs) should be 7mils.
5. Inter Pair spacing (spacing between one differential pair and another) should be a minimum of 20 mils except in the area near the pins.
6. Difference in trace lengths between "+" and "-" pairs should be within 5mils.
7. Difference in trace lengths among Inter pairs should be within 10mils.
8. "+" And "-" pairs should be routed in parallel.

2.7 Other function pins

• GLED, OLED

GLED and OLED pins output LED control signals to determine if the CH7511B/7512B is in normal or abnormal power and mode status. If GLED has output (3.3V), the CH7511B/7512B is in normal status. If OLED has output (flickers from 0 or 3.3V), the CH7511B/7512B is in abnormal status. The design is shown in Figure 7.

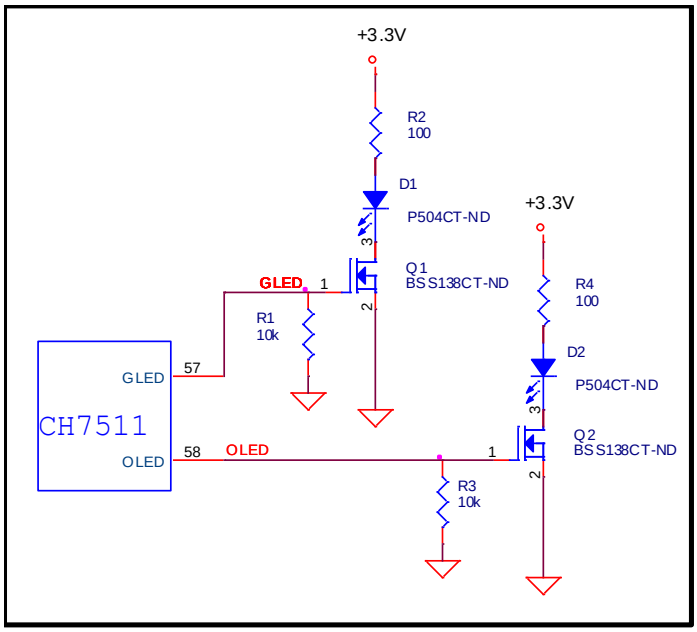


Figure 7: LED Control

• BLUP, BLDN

1. BLUP is the increase backlight brightness input pin.
2. BLDN is the decrease backlight brightness input pin.

Buttons can be placed at these pins to adjust the backlight brightness. The design is shown in Figure 8.

• PWRDN

The CH7511B/7512B enters into or exits power down state when receiving an active low pulse from this pin. The connection is shown in Figure 8.

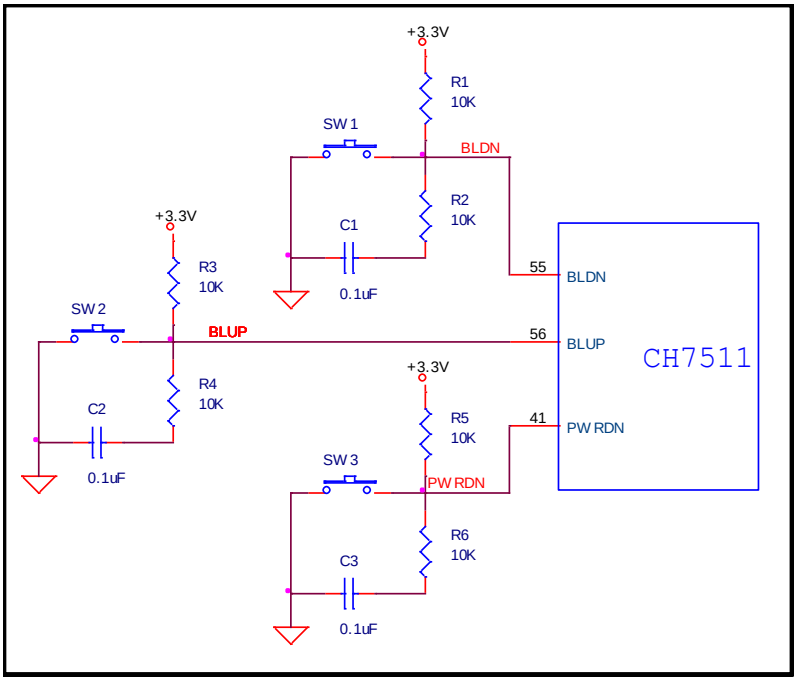


Figure 8: BLDN, BLUP and PWRDN Connections

• GPIO [0:3]

These pins can be used as panel select signals. They can be pulled high or low forming into 16 different combinations. Every combination can match with one panel type. The connection is shown in Figure 9.

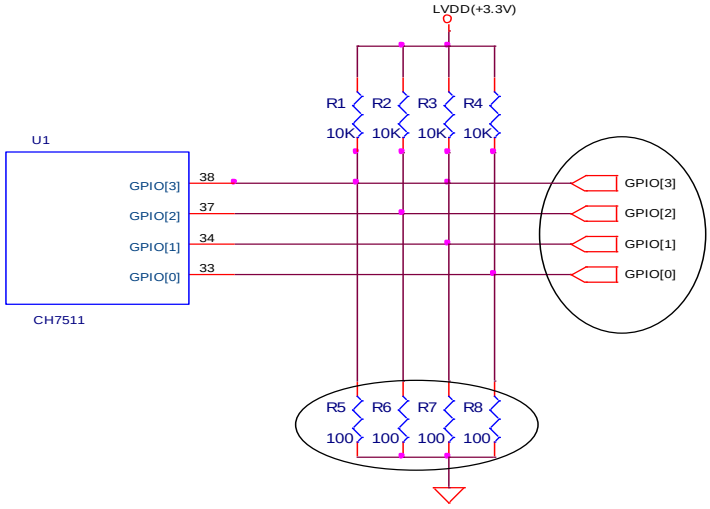


Figure 9: GPIO [0:3] connections

Method 1 (default)

GPIO [3:0] can be connected to high/low level by pull-up/pull-down resistors on the CH7511B/7512B PCB board; The CH7511B/7512B can obtain the correct LVDS Panel selection value upon power ON or reset. As shown in Figure 10, if the customer don't want to change MB, they can they the GPIO[0:3] in LCD inverter to identify different panel.

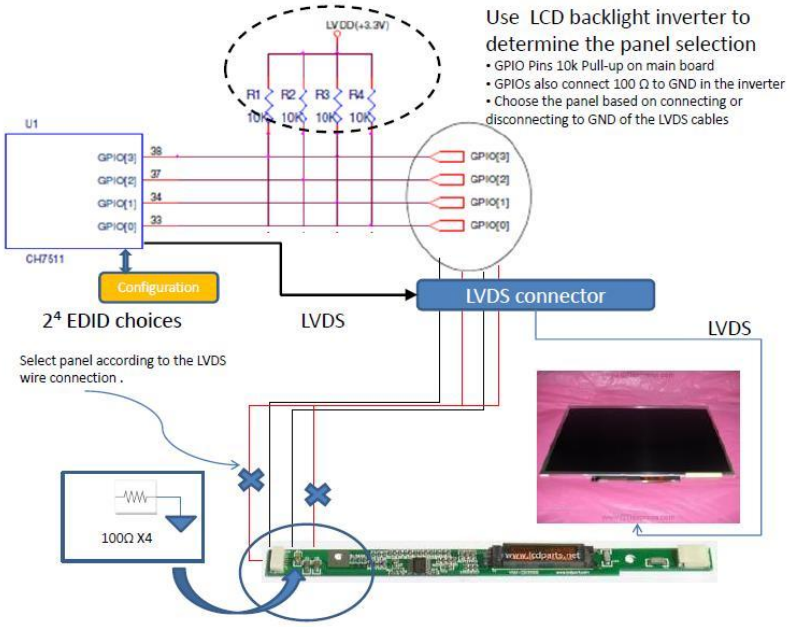


Figure 10: Typical application to control the CH7511B/7512B GPIO[3:0]

Method 2

GPIO [3:0] can be controlled by another chip's GPIO pins in the CH7511B/7512B application system. If the chip controlling the CH7511B/7512B GPIO [3:0] cannot set the expected value before the CH7511B/7512B finishes loading its firmware (typically 100ms after the CH7511B/7512B is powered ON), the controlling chip must reset the CH7511B/7512B for it to load the Boot ROM file again. It is recommended that the CH7511B/7512B be reset by the controlling chip each time the LVDS Panel selection value is changed.

Figure 11 shows the typical cases to control the CH7511B/7512B GPIO [3:0] by another chip. Case 1 is the right loading case, in which the GPIO pins remains stable within 100ms after reset. Case 2 is the wrong loading case, in which the GPIO value, represented by the GPIO pins, is still at random after the firmware is completely loaded. Therefore, the reset signal must be given again. The reset pulse width of larger than 10ms is recommended.

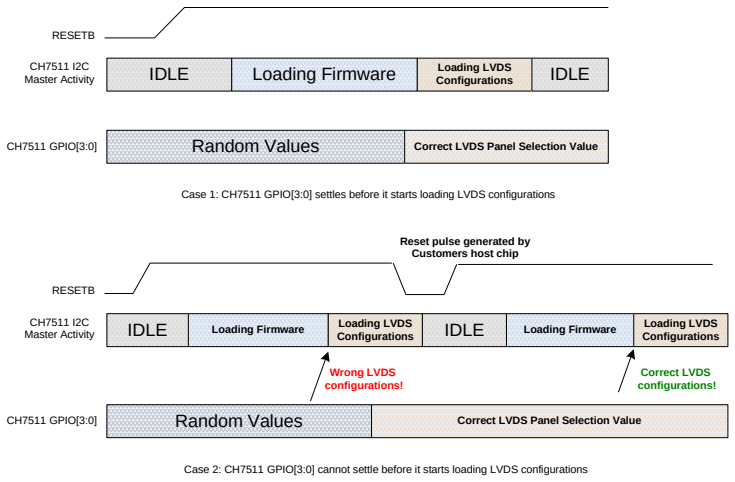


Figure 11: Typical cases to control CH7511B/7512B GPIO [3:0] by host chip

Note:

1. **The GPIO pins must remain stable for its corresponding value within 100ms after reset. Otherwise, a reset signal must be given again.**
2. **The firmware loading must be completed before VBIOS starts to function. Otherwise, some BIOS images may be lost.**

• PWM_OUT0, PWM_OUT1

The output Frequency from PWM_OUT0 can be up to 400 KHz. Its duty cycle ranges from 0% to 100%. Alternatively, the PWM bypass mode may be used to output the PWM signal through this pin. The voltage level is 3.3V.

The output Frequency from PWM_OUT1 can be up to 400 KHz. Its duty cycle ranges from 30% to 100%. The voltage level is 3.3V.

Customers may choose PWM_OUT0 or PWM_OUT1 in their application. Refer to the datasheet for detailed information.

• PWM_IN

PWM_IN has two working modes: Bypass mode and Duty Cycle Multiplication with AUX CH mode. In bypass mode, the input frequency to PWM_IN can be up to 1MHz. In Duty Cycle Multiplication with the AUX CH mode, the input frequency to PWM_IN can be up to 50 KHz. In either mode, the voltage level is 3.3V.

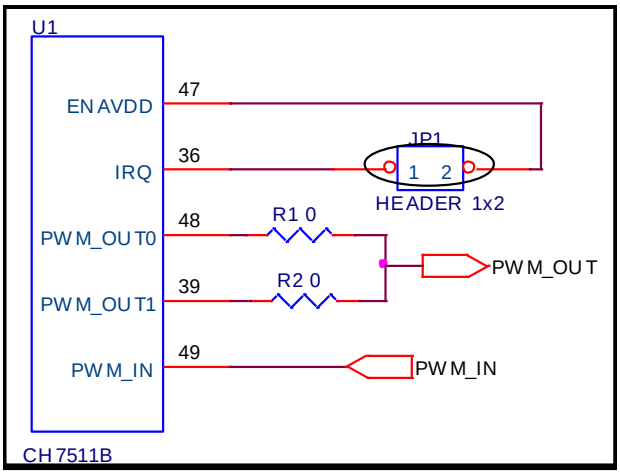


Figure 12: PWM and IRQ Control connections

• IRQ

IRQ (pin 36) can output an interrupt signal when the BLUP and BLDN are executing and should be connected to ENAVDD pin as shown in Figure 12.

• Reserved

Reserved pin (pin 2) should be left open in the application.

2.8 Important Design Considerations

(Panel power, backlight power, pull-up voltage)

• LVDS Power

Close attention must be paid to the power supplied to the LVDS backlight and the LVDS panel. Power requirements may differ from panel to panel. Please check the panels' power and backlight voltage specifications. The ENABKL and ENAVDD may be used to control the power for the LVDS backlight and the LVDS logic circuitry.

• Signal Wires, POWER and GND layout

Do not layout the wire or VIAs between the exposed thermal pad and the pin pads. Refer to Figure 13.

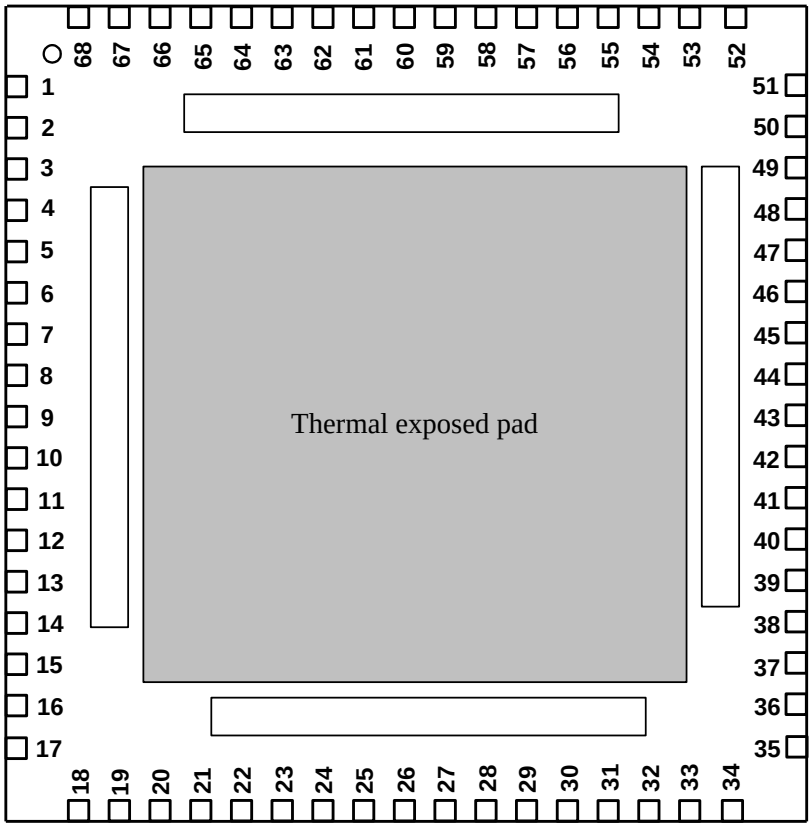


Figure 13: Wires or vias are not allowed in these four areas

2.9 Thermal Exposed Pad Package

The CH7511B/7512B is available in a 68-pin QFN package with exposed thermal pad. The advantage of the exposed thermal pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed thermal pad package provides a means of reducing the thermal resistance of the CH7511B/7512B. Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed thermal pad of the package should be soldered to the PCB as shown in Figure 14.

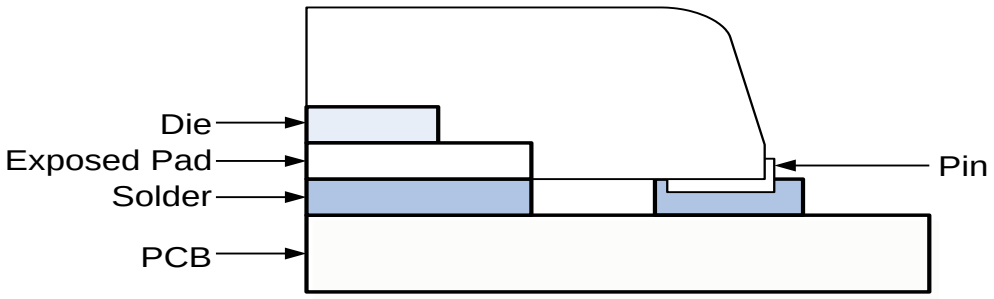
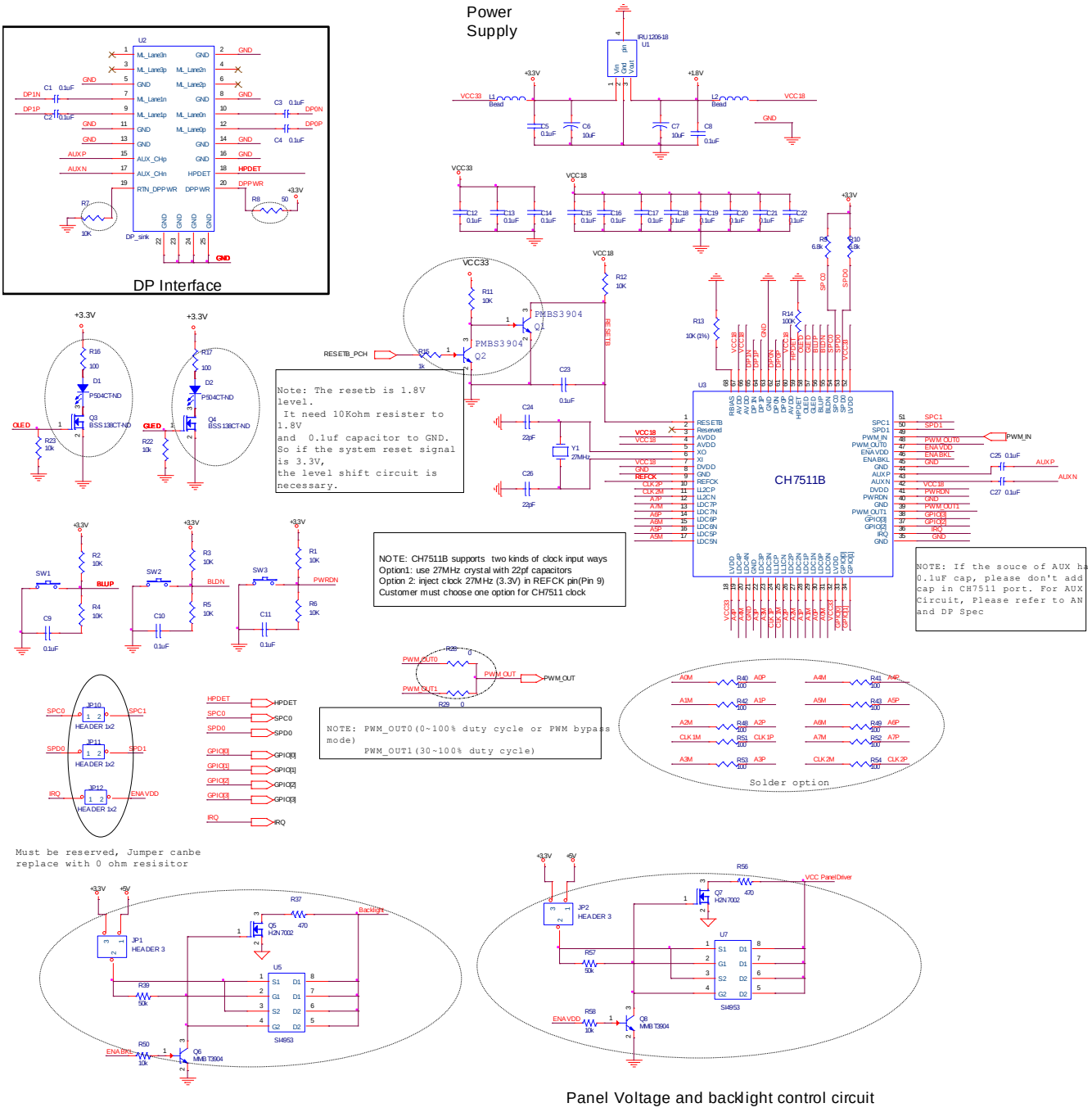


Figure 14: Cross-section of exposed thermal pad package

3.0 REFERENCE DESIGN EXAMPLE

The following schematics are to be used as a CH7511B/7512B PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7511B/7512B and would like to have a complete reference design schematic should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example



NOTE:
1. The dotted line parts are option funtion circuits.
2. The voltage circuit can only support CH7511B chip to work.If supporting the panel voltage, please add the other circuit.
3. Whether to use PWM_IN(3.3V), PWM_OUT0(3.3V) and PWM_OUT1(3.3V) is determined by customers. Which is used for Panel luminance adjustment.
4. DP and LVDS diffential pairs should be as short as possible. Please see appliciton note for detial layout guide
5. The CH7511B thermal exposed pad must be linked to GND

Figure 13: CH7511B/7512B Reference schematic

3.2 Reference Board Preliminary BOM

Table 2: CH7511B/7512B Reference Design BOM List

Item	Quantity	Reference	Part
1	23	C1, C2, C3, C4, C5, C8, C9, C10, C11, C12, C13, C15, C16, C17, C18, C19, C20, C21, C22, C23, C25, C27	0.1uF
2	2	C6, C7	10uF
3	2	C24, C26	22pF
4	2	D1, D2	P504CT-ND
5	2	JP1, JP2	HEADER 3
6	3	JP10, JP11, JP12	HEADER 2
7	2	L1, L2	Bead
8	2	Q1, Q2	PMBS3904
9	2	Q3, Q4	BSS138CT-ND
10	2	Q5, Q7	H2N7002
11	2	Q6, Q8	MMBT3904
12	17	R1, R2, R3, R4, R5, R6, R7, R11, R12, R18, R19, R20, R21, R22, R23, R50, R58	10K
13	1	R8	50
14	7	R9, R10, R32, R33, R34, R36, R38	6.8k
15	1	R13	10K(1%)
16	1	R14	100K
17	1	R15	1K
18	16	R16, R17, R24, R25, R26, R27, R40, R41, R42, R43, R48, R49, R51, R52, R53, R54,	100
19	1	R35	1.8k
20	2	R37, R56	470
21	2	R39, R57	50k
22	2	R28, R29	0
23	3	SW1, SW2, SW3	P8058SS-ND
24	1	U1	IRU1206-18
25	1	U2	DP_Sink
26	1	U3	CH7511B/7512B
27	1	U4	CH9904 (SOIC-8)
28	2	U5, U7	SI4953
29	1	Y1	27MHz

4.0 REVISION HISTORY

Table 3: Revisions

Rev. #	Date	Section	Description

1.0	04/19/2012	All	Layout Guide and Design Guide for CH7511B and CH7512B release.
1.1	11/29/2013	2.3 2.5	Add demand of RBIAS Add demand of DP layout
1.2	03/11/2014	2.5 3.1	Modify Aux reference schematic Update reference schematic
1.3	10/13/2014	2.4 2.6 2.7 3.1	Modify SPC0, SPC1, SPD0, SPD1 schematic Modify demand of LVDS layout rules Modify IRQ schematic Update reference schematic
1.4	11/11/2014	All	Technical and grammatical review
1.5	01/27/2015	2.4	Modify description of SPC1 and SPD1
1.6	04/18/2016	2.3 2.4	Modify Reset Modify SPC1 and SPD1
1.7	07/14/2020	Disclaimer	Update the disclaimer

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