CH7518 DisplayPort to BT656 Converter

FEATURES

- Compliant with DisplayPort specification version 1.2 and Embedded DisplayPort (eDP) specification version 1.3.
- Support 2 Main Link Lanes at either 1.62Gb/s or 2.7Gb/s link rate
- Support ITU-R 601 or ITU-R 656 compatible YCbCr 4:2:2 output format with embedded syncs or discrete syncs. Support resolution up to 1280 x 720@60Hz for YCbCr 4:2:2 output
- HDCP engine compliant with HDCP 1.3 specification with internal HDCP Keys
- On-chip Audio Decoder which support 2 channel IIS/ S/PDIF audio output
- Support RGB to YCC conversion in ITU-R BT.601 and 709 color space
- Embedded MCU to handle the control logic
- Support device boot up by automatically loading firmware from on-chip flash Boot ROM
- Integrated EDID Buffer
- Supports Enhanced Framing Mode
- Fast and full Link Training for embedded DisplayPort system
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- 2 work modes: connect 27MHz crystal, inject 27MHz clock
- DP input detection supported
- Support RGB to YCC conversion in ITU-R BT.601 and 709 color space
- Support Auto Power Saving mode and low stand-by current
- Support Spread Spectrum Clocking (de-spreading) for EMI reduction
- DP AUX channel and IIC slave interface are available for firmware update and debug
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 40-Pin QFN package (6 x 6 mm)

APPLICATION

- Car Entertainment Device
- Notbook/Ultrabook
- Tablet Device
- Handheld/Portable Device

GENERAL DESCRIPTION

Chrontel's CH7518 is a low-cost, low-power semiconductor device that translates the DisplayPort signal to the BT656 or 8 bit YCbCr 4:2:2 signal. This innovative DisplayPort receiver with an integrated BT656 encoder is specially designed to target the Notebook/Ultrabook, tablet device and automobile entertainment device. Through the CH7518's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized multimedia data can be seamlessly converted to BT656 video and IIS or SPDIF audio output.

The CH7518 is compliant with the DisplayPort Specification 1.2 and the Embedded DisplayPort Specification version 1.3. With internal HDCP key Integrated, the device support HDCP 1.3 specifications. In the device's receiver block, which supports two DisplayPort Main Link Lanes input with data rate running at either 1.62Gb/s or 2.7Gb/s, can accept RGB digital formats in either 18-bit 6:6:6 or 24-bit 8:8:8, and converted the input signal to 8 bit YCbCr output signal up to 1280 x 720@60Hz. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7518 is capable of instantly bring up the video display to the device of BT656 input when the initialization process is completed between CH7518 and the graphic chip.

With sophisticated MCU and the Boot ROM embedded, CH7518 support auto-boot and EDID buffer. After the configuration by firmware, which is auto loaded from Boot ROM, CH7518 can support DP input detection, and determine to enter into Power saving mode automatically.

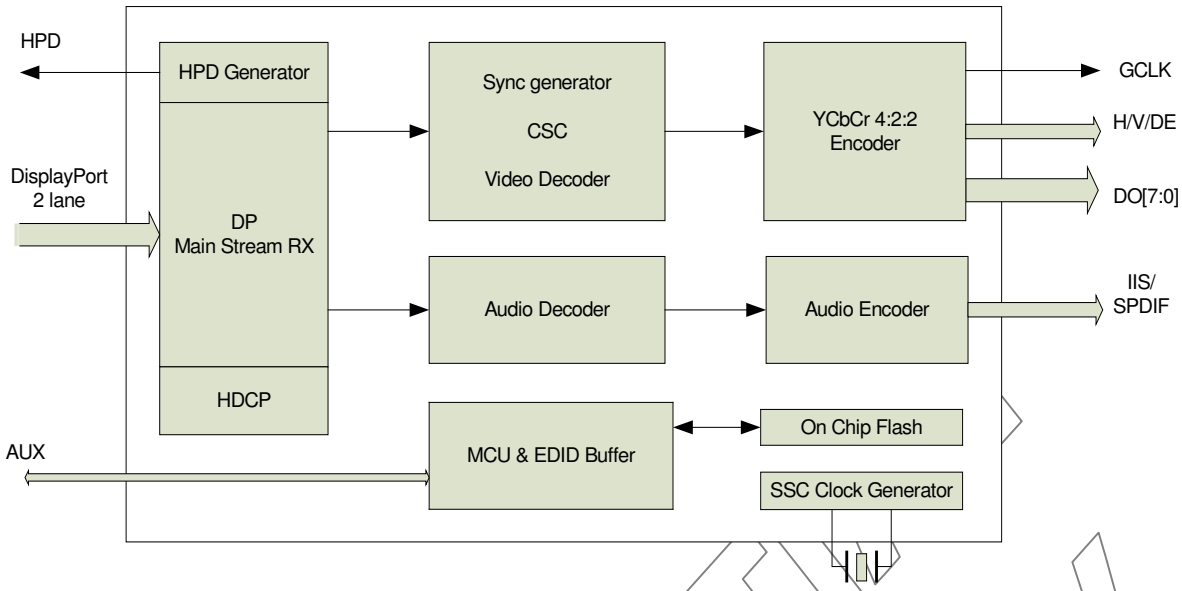

Figure 1: CH7518 Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

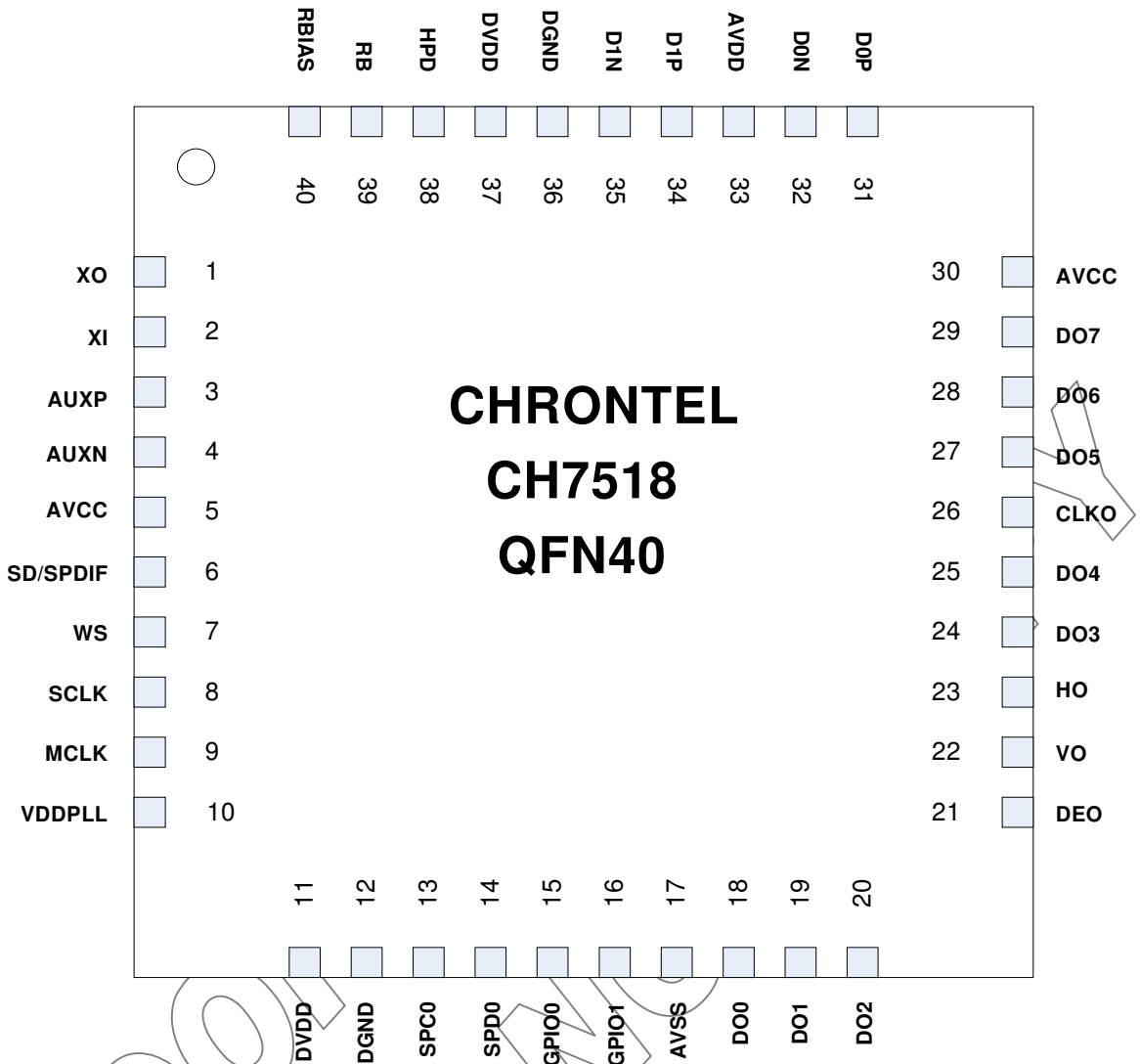

Figure 2: CH7518 40-pin QFN pin out

1.2 Pin Description

Table 1: Pin Name Descriptions

Pin #	Type	Symbol	Description
1	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open
2	In	XI	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI Input
3,4	In/Out	AUXP/N	**DP AUX Channel Differential Input/Output** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
6	Out	SD/SPDIF	**I2S Serial data or SPDIF Output**
7	Out	WS	**I2S Word Select**
8	Out	SCLK	**I2S Continuous Serial Clock**
9	Out	MCLK	**I2S System Clock**
13	In	SPC0	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
14	In/out	SPD0	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required
15,16	In/Out	GPIO[1:0]	**General Purpose Input/Output**
18~20,24,25,27~29	Out	DO0~DO7	**BT656 Data Output**
21	Out	DEO	**Data Enable Output of BT656**
22	Out	VO	**VSYNC Output of BT656**
23	Out	HO	**HSYNC Output of BT656**
26	Out	CLKO	**Clock Output of BT656**
31,32,34,35	In	DP[1:0]P/N	**DP Main Link Differential Line Input** These pins accept two AC-coupled differential pairs signals from the DisplayPort transmitter.
38	Out	HPD	**DP Receiver Hot Plug Output**
39	In	RB	**Chip Reset** Low to 0V for reset. Typical High level is 3.3V
40	In	RBIAS	**Current Set Resistor Input** This pin sets the DAC current. A 1.2 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces.
5,30	Power	AVCC	**Analog Power Supply (3.3V)**
10	Power	VDD_PLL	**PLL Power Supply (1.2V)**
11,37	Power	DVDD	**Digital Core/IO Power Supply (1.2V)**
12,36	Power	DGND	**Digital Ground**
33	Power	AVDD	**Analog Core Power Supply (1.2V)**
17, pad	Power	AVSS	**Analog Ground**

2.0 PACKAGE DIMENSION

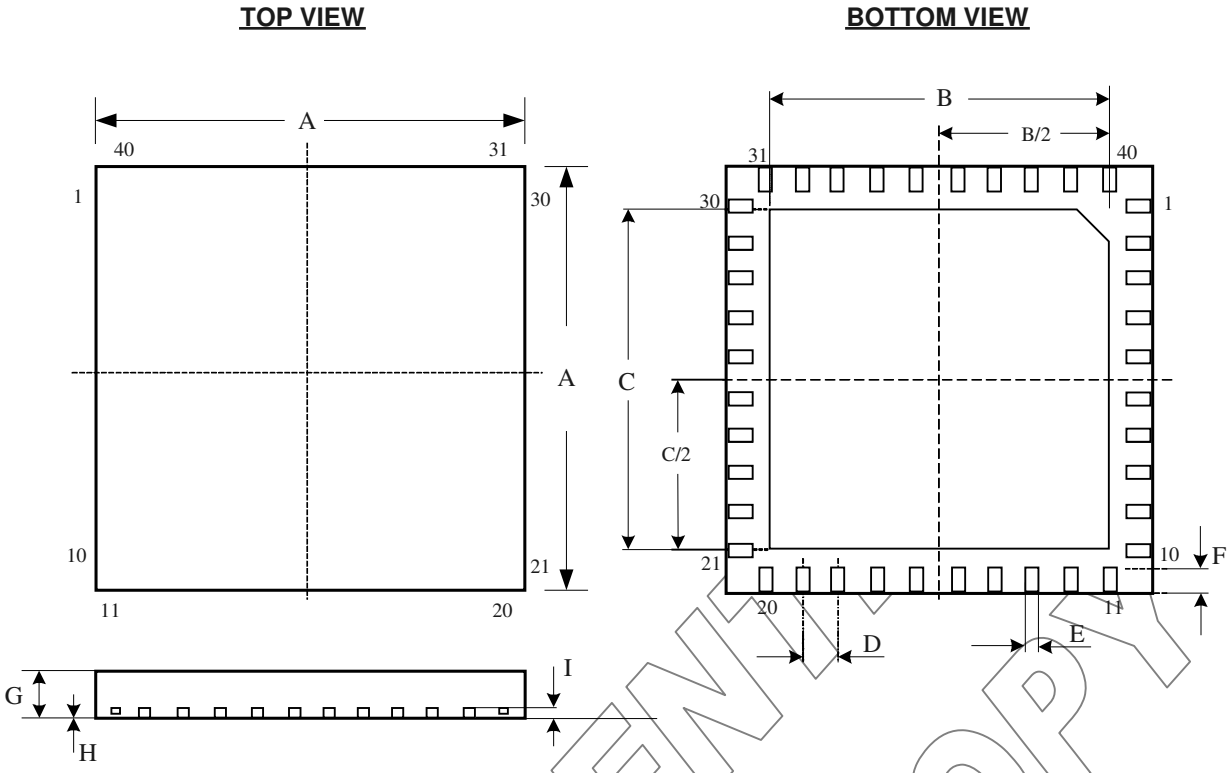

Figure 3: 40 Pin QFN Package

Table of Dimensions

No. of Leads		SYMBOL								
40 (6 X 6 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	5.90	4.40	4.40	0.5	0.18	0.30	0.80	0	0.203
	MAX	6.10	4.60	4.60		0.30	0.50	0.90	0.05	

Notes:
Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION

Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7518A-BF	40 QFN, Lead-free	Commercial : -20 to 70°C	490/Tray
CH7518A-BFI	40 QFN, Lead-free	Industrial : -40 to 85°C	490/Tray

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