CH7519 DisplayPort to HDTV Converter

FEATURES

- Compliant with DisplayPort(DP) specification version 1.2
- Support 2 Main Link Lanes at either 1.62Gb/s or 2.7Gb/s link rate
- Support HDTV format (YPbPr output) for 480p, 576p, 720p, 1080i and 1080P
- HDCP engine compliant with HDCP 1.3 specification with internal HDCP Keys
- On-chip Audio Decoder which support 2 channel IIS/ S/PDIF audio output
- Embedded MCU to handle the control logic
- Support device boot up by automatically loading firmware from on-chip flash Boot ROM
- Integrated EDID Buffer
- Supports Enhanced Framing Mode
- 2 work modes: connect 27MHz crystal, inject 27MHz clock
- TV connection detection supported
- DP input detection supported
- Support RGB to YCC conversion in ITU-R BT.601 and 709 color space
- Support Auto Power Saving mode and low stand-by current
- Support Spread Spectrum Clocking (de-spreading) for EMI reduction
- DP AUX channel and IIC slave interface are available for firmware update and debug
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 40-Pin QFN package (6 x 6 mm)

APPLICATION

- Car Entertainment Device
- DP to YPbPr Adapter/Docking Station
- Notbook/Ultrabook
- Tablet Device
- Handheld/Portable Device
- PC

GENERAL DESCRIPTION

Chrontel's CH7519 is a low-cost, low-power semiconductor device that translates the DisplayPort signal to the YPbPr . This innovative DisplayPort receiver with integrated HDTV encoder and three separate 9-bit video Digital-to-Analog Converters (DACs) is specially designed to target the DisplayPort Docking Station, Automobile Entertainment Device, Notebook/Ultrabook and PC market segments. Through the CH7519 's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized multimedia data can be seamlessly converted to HDTV video and IIS or SPDIF audio output.

The CH7519 is compliant with the DisplayPort Specification 1.2. With internal HDCP key Integrated, the device support HDCP 1.3 specifications. In the device's receiver block, which supports two DisplayPort Main Link Lanes input with data rate running at either 1.62Gb/s or 2.7Gb/s, can accept RGB digital formats in either 18-bit 6:6:6 or 24-bit 8:8:8, and converted the input signal to YPbPr. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7519 is capable of instantly bring up the video display to the analog HDTV when the initialization process is completed between CH7519 and the graphic chip.

The DACs are based on current source architecture. With sophisticated MCU and the Boot ROM embedded, CH7519 supports auto-boot and EDID buffer. After the configuration by firmware, which is auto loaded from Boot ROM, CH7519 can support DP input detection, TV connection detection, and determine to enter into Power saving mode automatically.

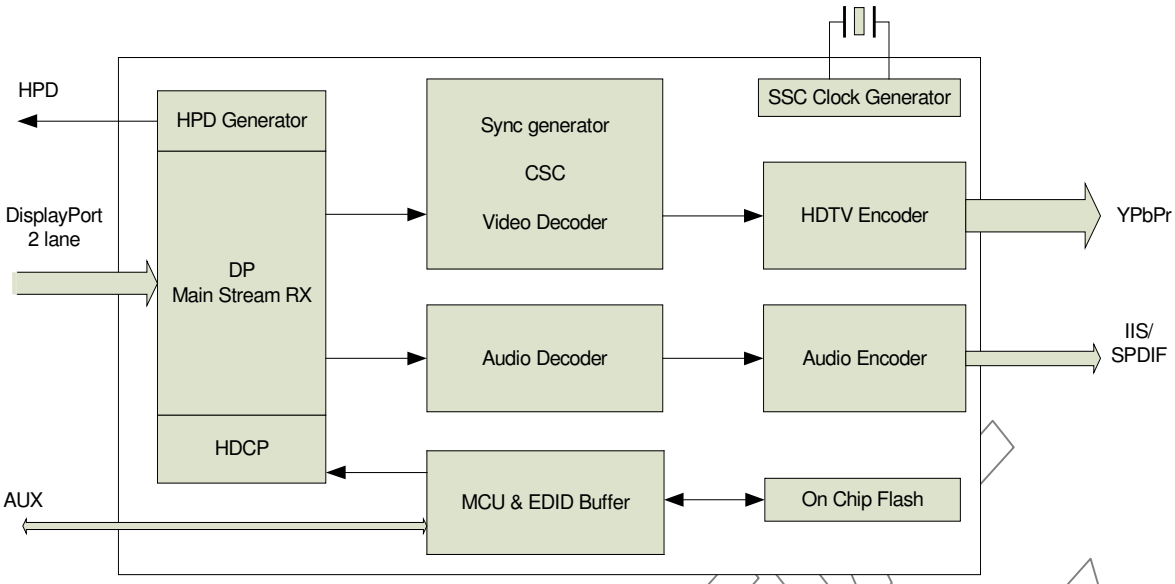

Figure 1: CH7519 Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

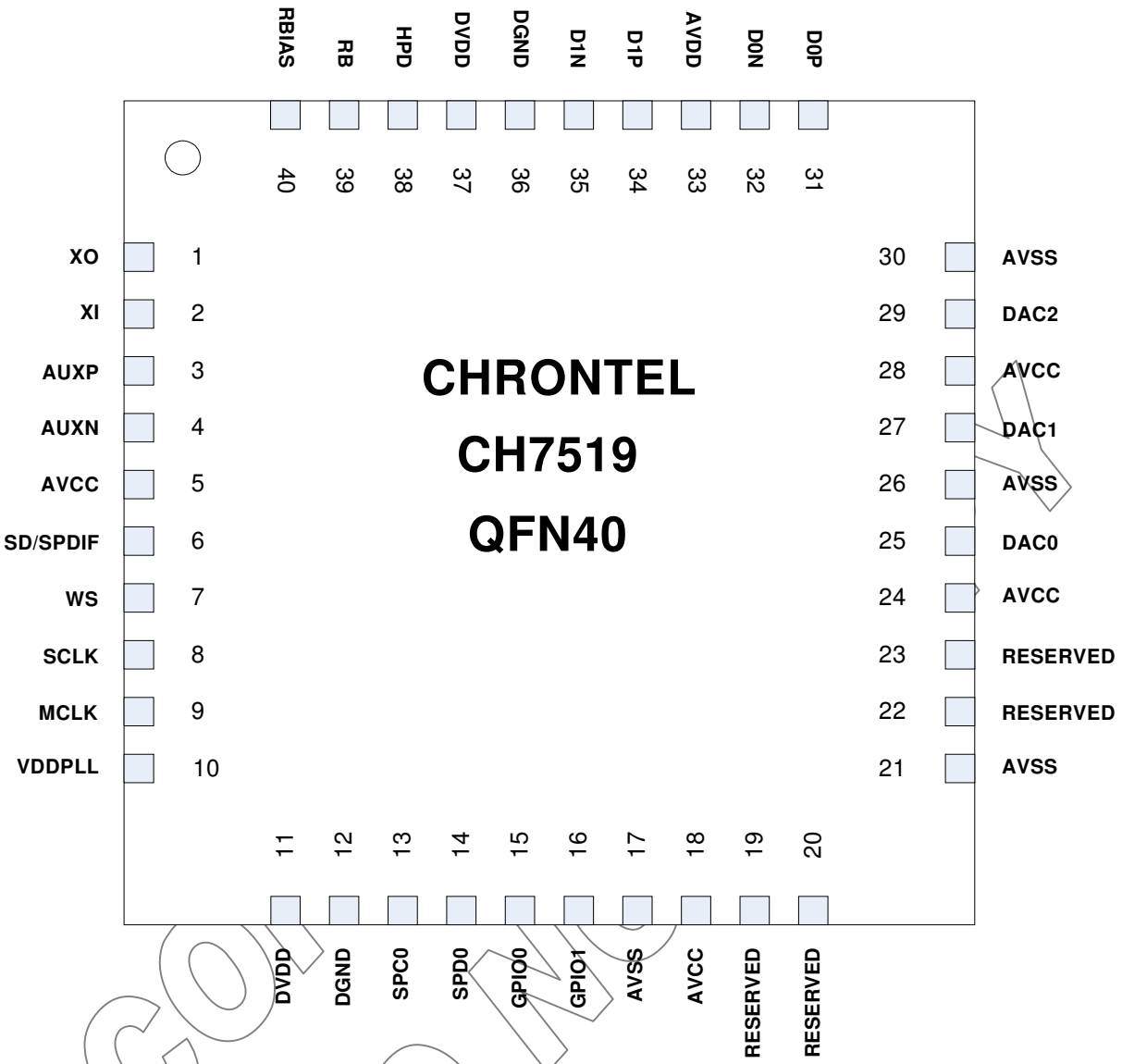

Figure 2: CH7519 40-pin QFN pin out

1.2 Pin Description

Table 1: Pin Name Descriptions

Pin #	Type	Symbol	Description
1	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open.
2	In	XI	**Crystal Input** A parallel resonance crystal should be attached between this pin and XO.
3,4	In/Out	AUXP/N	**DisplayPort AUX Port** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
6	Out	SD/SPDIF	**I2S Serial Data or SPDIF Output**
7	Out	WS	**I2S Word Select**
8	Out	SCLK	**I2S Continuous Serial Clock**
9	Out	MCLK	**I2S System Clock**
13	In	SPC0	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
14	In/out	SPD0	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required
15,16	In/Out	GPIO[1:0]	**General Purpose Input/Output**
19,20,22,23		RESERVED	**Reserved Pins** These pins should be left open in the application
25	Out	DAC0	**HDTV Pr Component Output**
27	Out	DAC1	**HDTV Pb Component Output**
29	Out	DAC2	**HDTV Y Component Output**
31,32,34,35	In	D[1:0]P/N	**DP Rx Input Lane 1 and Lane 0**
38	Out	HPD	**DP Receiver Hot Plug output**
39	In	RB	**Chip Reset** Low to 0V for reset. Typical High level is 3.3V
40	In	RBIAS	**Current Set Resistor Input** This pin sets the DAC current. A 10KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces
5,18,24,28	Power	AVCC	**Analog Power Supply (3.3V)**
10	In	VDDPLL	**PLL Power Supply (1.2V)**
11,37	Power	DVDD	**Digital Power Supply (1.2V)**
12,36	Power	DGND	**Digital Ground**
17,21,26,30 ,pad	Power	AVSS	**Analog Power Ground**
33	Power	AVDD	**Analog Power Supply (1.2v)**

2.0 PACKAGE DIMENSION

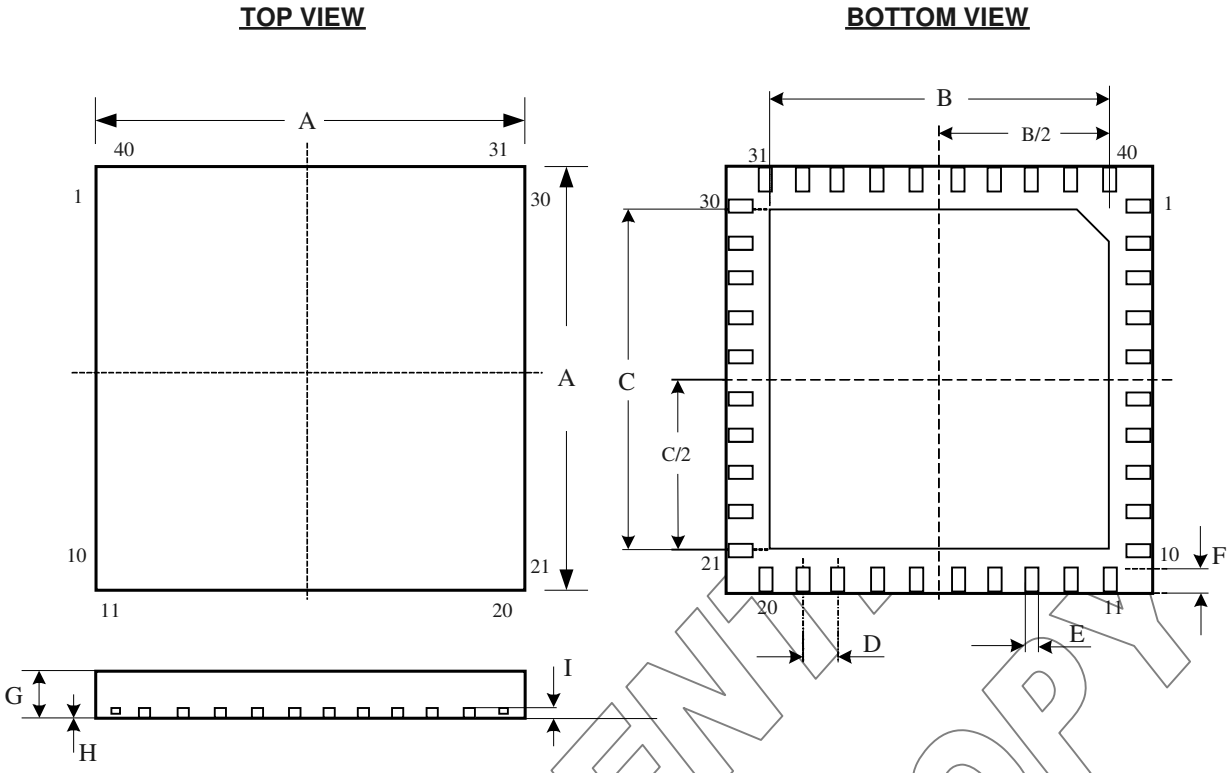

Figure 3: 40 Pin QFN Package

Table of Dimensions

No. of Leads		SYMBOL								
40 (6 X 6 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	5.90	4.40	4.40	0.5	0.18	0.30	0.80	0	0.203
	MAX	6.10	4.60	4.60		0.30	0.50	0.90	0.05	

Notes:
Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION

Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7519A-BF	40 QFN, Lead-free	Commercial : -20 to 70°C	490/Tray
CH7519A-BFI	40 QFN, Lead-free	Industrial : -40 to 85°C	490/Tray

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