PCB Layout and Design Guide for CH7530

DP++ to HDMI/DVI Level Shifter

1.0 INTRODUCTION

Chrontel's CH7530 is a low-cost, low-power semiconductor device that translates the DisplayPort dual mode signal to HDMI/DVI signal. This innovative device, which integrates programmable equalizer, high speed TMDS level shifter and IIC to AUX translator, is specially designed to target the DP++ to HDMI/DVI adaptor device, docking station and PC market segments

The CH7530 is compliant with the DisplayPort dual mode standard specification version 1.1. With sophisticated equalizer and high-speed TMDS level shifter integrated, the device's TMDS signal output is compliant with HDMI specification version 1.4b and DVI specification version 1.0, and supports video resolution up to 4Kx2K@30Hz or 1920x1080@120Hz for 3D applications. The CH7530 also integrates the HDMI identifier, IIC over AUX translator and the related DDC control registers, which enables the programmable HDMI or DVI output and supports both DDC and AUX signaling on the upstream DisplayPort connector. With step-up regulator integrated, CH7530 supports 5V power supply output for HDMI/DVI configuration

This application note focuses only on the basic PCB layout and design guidelines for CH7530. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 40-pin QFN package of the CH7530A-BF GBE. Please refer to the CH7530 datasheet for the details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7530 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply and Decoupling

2.1.1 Charge Pumper & LDO

To provide the highest level of integration in external adapter applications, CH7530 includes an internal 3.3V to 5V charger pumper and a 3.3V to 1.2V LDO.

The output of charger pumper is designed to provide maxim 55mA 5 V power supply to the DVI or HDMI connector. It required one external 1uF capacitors between pin PCP and pin PCN to operate. The output pin V5OUT required a 10uF capacitor to ground as shown in **Figure 1**. Its output is active whenever a valid 3.3V is applied to the CH7530 AVCC. If the internal charger pumper of CH7530 is not used, the 1uF capacitor between pin PCP and pin PCN shall not be used.

The internal LDO is active whenever a valid 3.3V is applied to the CH7530 AVCC and the pin DDC_MOD is pulled to AVCC.

When you want to use the external power supply, you have to pull the pin DDC_MOD to ground or open-circuit. Please refer to the reference schematic for the circuit details.

The power consumption is different, when we use internal LDO or external DC-DC. A typical test data is listed in the **Table 1**.

Table 1：Power consumption of different power supply mode

mode	DP++ input(3.3V)	HDMI input(5V)	mode	DP++ input(3.3V)	HDMI input(5V)
internal LDO	125mA	117mA	external DC-DC	80mA	75mA
power consumption	0.4125mW	0.585mW	power consumption	0.264mW	0.375mW

2.1.2 Ground Pins & Power Supply Pins

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7530 ground pins, in addition to ground vias.

The CH7530 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7530 ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 2** for the Ground pins assignment.

Refer to **Table 2** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 2: Power Supply Pins Assignment of the CH7530 (QFN48)

Pin Assignment	# of Pins	Type	Symbol	Description
1,20	2	Power	VCC12	Analog Power Supply (1.2V) with internal LDO
6,19,23,28,38	5	Power	AVCC	Analog Power Supply (3.3V)
41	1	Ground	Thermal Pad	Power supply ground

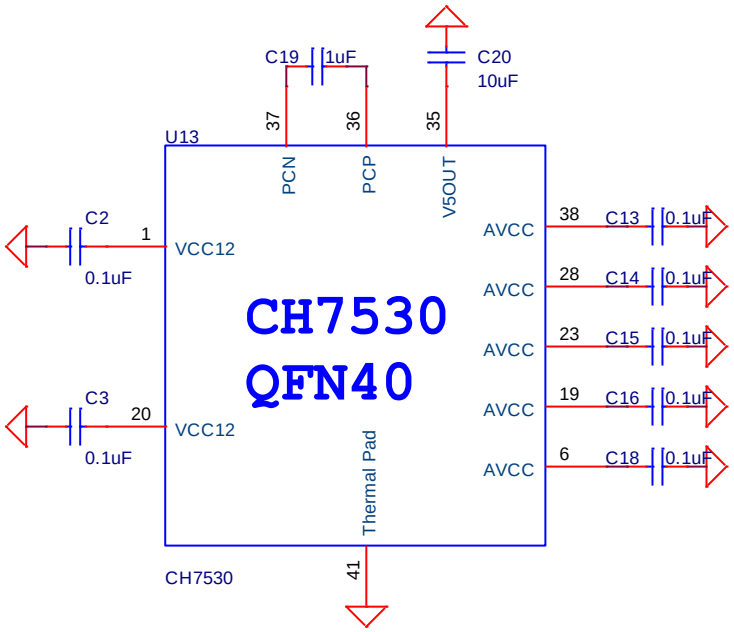

Figure 1: Power Supply Decoupling and Distribution

2.1.3 Power On Timing

There're two kinds of power supply configurations for CH7530, one is using the external 3.3V and 1.2V power supply to power on CH7530, the other is using the external 3.3V power supply, and the internal 3.3V to 1.2V power regulator (LDO) by configuring the DDC_MOD pin.

While using the external 3.3V and 1.2V power supply, in order to make sure that CH7530 can work normally. The power on timing in **Figure 2** should be followed.

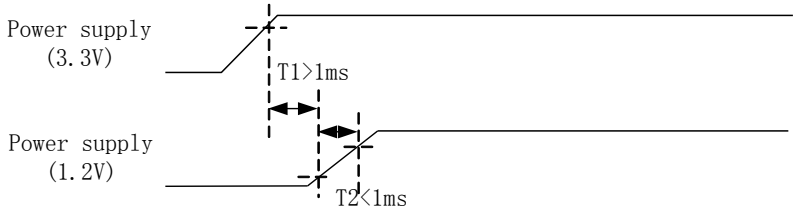

Figure 2: Power on timing

Note: 1. Power on wave shall be smooth.
2. 1.2V shall be delayed for more than 1ms to be turned on after 3.3V rises above 2.5V.
3. The rising time (0.1V~0.8V) of 1.2V power supply shall not exceed 1ms.

2.2 Internal Control Pins

• VSWING Pin

This pin sets the swing level of the HDMI/DVI outputs. A 11.5kΩ with 1% tolerance resistor should be connected between this pin and GND using short and wide traces.

• DDC_EN Pin

This pin enables the DDC buffer and level shifter. When DDC_EN = LOW, buffer/level shifter is disabled.

When DDC_EN = HIGH, buffer and level shifter are enabled .To prevent the back drive from sink via DDC channel.

This pin requires a pull-up 10kΩ resistor to AVCC as shown in **Figure 3**. The default setting is 10k to AVCC.

• DDC_MOD Pin

It provides DDC buffer configuration and control the internal LDO power on or power down, the details are as follow **Table 3**. This pin can be board-strapped to one of five decode values as shown in **Figure 3**. The default setting is 22k to AVCC.

Table 3: Pin DDC_MOD Configuration

Options	Short to AVCC	22k to AVCC	OPEN CIRCUIT	22k or short to GND
DDC buffer	Active buffer	Passive buffer	Active buffer	Passive buffer
PD_LDO	0	0	1	1

• CFG Pin

This pin control the HDMI/DVI output selection, when CFG=HIGH, HDMI output is selected, when CFG=LOW, DVI output is selected as shown in **Figure 3.** The default setting is 10k or short to AVCC.

• PREEM Pin

It controls Pre-emphasis Driver Setting as follow **Table 4.** This pin can be board-strapped to one of five decode values as shown in **Figure 3**. The default setting is open-circuit.

Table4: Pin PREEM Driver Setting

Options	Short to AVCC	22k to AVCC	OPEN CIRCUIT	22k to GND	Short to GND
Driver Setting	0dB	3dB	5dB	7dB	10dB

• EQ Pin

This pin control Programmable Equalizer Setting as follow **Table 5.** This pin can be board-strapped to one of five decode values as shown in **Figure 3.** The default setting is 22kΩ resistor to AVCC.

Table5: Pin EQ Equalizer settings9

Options	Short to AVCC	22k to AVCC	OPEN CIRCUIT	22k to GND	Short to GND
Equalizer settings	1dB	4dB	7dB	10dB	13dB

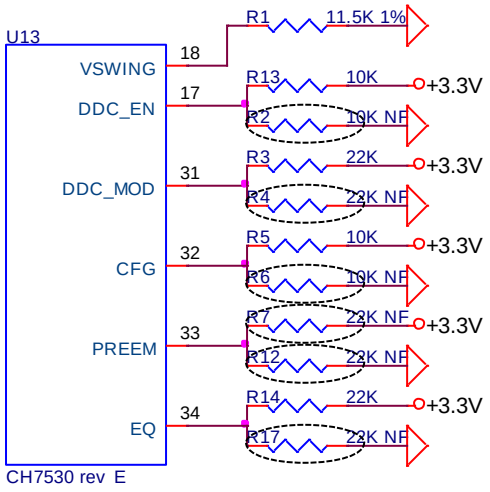

Figure 3: Internal Control Pins

2.3 Display Port + + Signal Pins

• DP0P/N, DP1P/N, DP2P/N, DP3P/N

These pins accept four differential pairs of signals from the DisplayPort++ transmitter. When CH7530 is used for Apple Mac book, AC-coupled capacitors are recommended to be used. DP++ signal input connection shown in the **Figure 4**. When CH7530 is used for HDMI extender, HDMI signal input connection is shown in the **Figure 5**.

These signals are high speed differential signal. Please refer to the section 2.5 for layout guide.

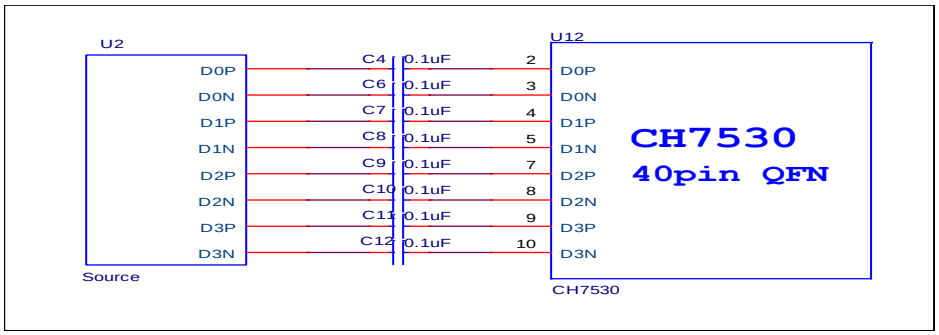

Figure 4: CH7530 DP++ Input

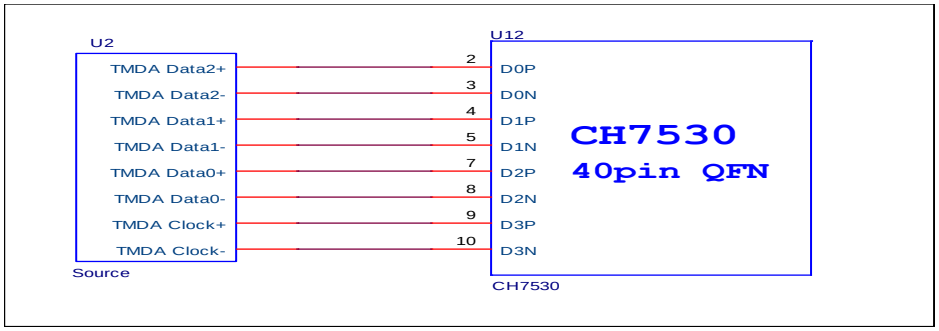

Figure 5: CH7530 HDMI Input

• AUXP and AUXN

The CH7530 is in compliance with DisplayPort Dual mode Specification version 1.1. The AUX RX embedded in The CH7530 only responds to IIC-over-AUX transactions. The CH7530 is bridge convert one or multiple IIC-over-AUX transactions to a single IIC transaction. The converting function from AUX to IIC can be processed by Hardware mode. This AUX pair needs to be pulled up to 3.3V through 2K resistors.

• HPD and CEC_SC

This output pin indicates whether this device is active or not. It is buffer output of HPD in. Output voltage is 3.3V. A resistor more than 100K-Ohm should be connected between this pin and GND. The CEC pin to DP dual mode required a 27K resistor to AVCC as shown in **Figure 6**.

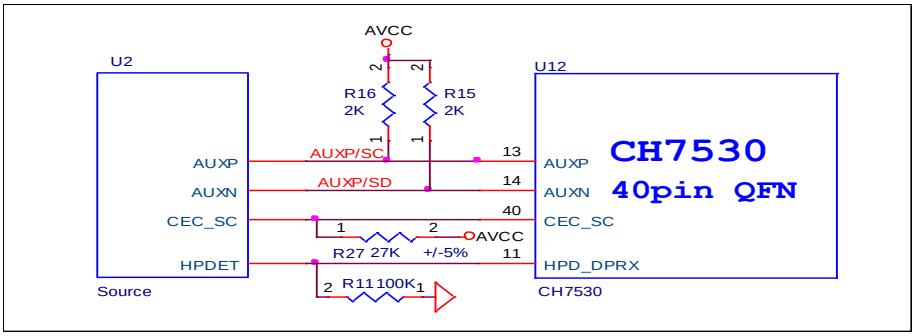

Figure 6: CH7530 AUX channel and HPD

2.4 HDMI Output Pins

• TXC-/TXC+, TX0-/TX0+, TX1-/TX1+, TX2-/TX2+

The TXC-/TXC+, TX0-/TX0+, TX1-/TX1+, TX2-/TX2+ signals are high frequency differential signals that need to be routed with special precautions. Since those signals are differential, they must be routed in pairs.

These signals are high speed differential signal, please refer to the section 2.5 for layout guide.

• HPD_HMTX

This output pin connects to the GND through a 47KΩ resistor. Refer to **Figure 7** for the design example.

• CEC_SK

The CEC_SK is CEC pin to HDMI sink.

• DDC_SCL and DDC_SDA

DDC_SCL and DDC_SDA are used to interface with the DDC of HDMI source. The DDC is used by CH7530 to tell source the capabilities and characteristics of the CH7530 by transfer the E-EDID data. This DDC pair needs to be pulled up to 5V through 10K resistors and diodes as shown in **Figure 7**. The diode is used to avoid back drive from DDC signal.

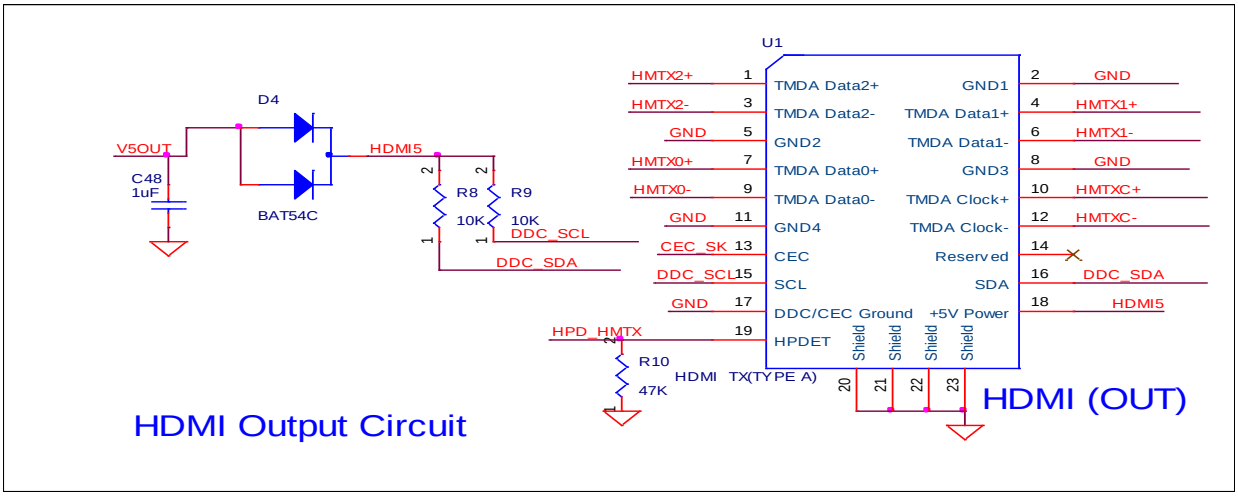

Figure 7: The connection of the HDMI outputs

2.5 DP++/HDMI differential pair signals layout

2.5.1 DP++/HDMI Differential Pair Impedance

To match the external cable impedance and maintain the maximal energy efficiency.It is important to meet the impedance target of 100-Ω ± 10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thickness, board dielectric, etc. The differential pairs should be routed on the top layer directly to the connector pads if possible. It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair.

2.5.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized, inductive effects may be introduced, causing spikes in the signals. Trace routing lengths from CH7530 to the input and output connector are limited to a maximum of 2 inches. The CH7530 should be as close to the connector as possible.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

Use the smallest size vias and connector pads. It is recommended that 12 mils inner diameter and 18 mils outer diameter vias or smaller one should be used in routing these signals. At most one via can be used on trace.

2.5.3 Trace Routing Length matching

It is recommended that length matching of both signals of a differential pair be within 5 mils. Length matching should occur on a segment-by-segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 100 mils.

2.5.4 Others

It is strongly recommended that the connection of these video signals between the graphics controller and the CH7530 should be kept as short as possible and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals.

The differential pairs should be placed above solid ground plane or power plane to minimize un-continued impedance.

2.6 Thermal Exposed Pad Package

The CH7530 is available in 40-pin QFN package with thermal exposed pad package. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7530.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 8**.

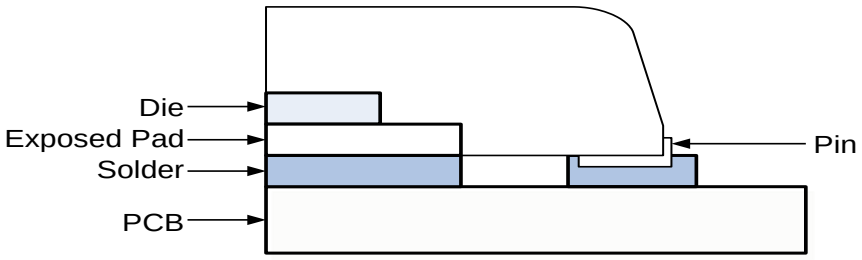

Figure 8: Cross-section of exposed pad package

BTW, for the assembly process, it is important to limit the amount of solder paste that is put under the thermal pad. If too much paste is put on the PCB, the package may float during assembly. Compared with the solder mask of thermal pad, the paste mask should be shrank to70%~80%.

3.0 REVISION HISTORY

Table5: Revisions

Rev. #	Date	Section	Description
0.1	3/31/2016	All	Initial Draft for CH7530
0.2	8/22/2016	Section 2.2	Add description for VSWING,
0.3	8/22/2016	Section 2.2	Modify the value of resistor
0.4	9/13/2016	Section 2.1	Modify PCN, PCP pin number
0.5	9/12/2018	Section 2.1	Modify PCN, PCP pin number
1.0	7/15/2020	Disclaimer	Update the Disclaimer

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