PCB Layout and Design Guide for CH7218

1.0 INTRODUCTION

Chrontel's CH7218A is a low-cost, low-power semiconductor device that translates the DisplayPort signal to HDMI 2.1 through the USB Type-C connector. The CH7218's DP/eDP receiver is compliant with the DisplayPort Specification 1.4 and Embedded DisplayPort (eDP) Specification version 1.4. With sophisticated DisplayPort signal detection and the Lane Swap/AUX polarity inversion logic, the CH7218 supports USB Type-C cable plug orientation switch. With internal HDCP key Integrated, the device support HDCP 2.3 specifications. In the device's receiver block, which supports four DisplayPort Main Link Lanes input with data rate running at 1.62Gbps, 2.7Gbps, 5.4Gbps or 8.1Gbps, and converted the input signal to HDMI output up to 8Kx4k@60Hz or 4K2K@120Hz in Fixed Rate Link mode. Leveraging the USB Power Delivery control logic, the USB billboard module for USB device indentify and DisplayPort's unique source/sink "Link Training" routine, the CH7218 is capable of instantly bring up the video display to the HDMI 2.1 TV/Monitor when the initialization process is completed.

This application note focuses only on the basic PCB layout and design guidelines for the CH7218. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures presented in this document are based on the 68-pin QFN (8x8 mm) package of the CH7218. Please refer to the CH7218 datasheet for details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7218 should be placed as close as possible to the respective pins. The following will describe guidelines on how to connect critical pins, as well as the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimal power supply decoupling is accomplished by placing a ceramic capacitor at each of the power supply pins as shown in Figure 1. These capacitors (C1, C2, C3, C4, C6, C7, C9, C11, C12, C14, C15, C16, C17, C18, C19 , and C21) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7218 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The CH7218 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7218 ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to Table 1 for the Ground pin assignments.

2.1.2 Power Supply Pins

There are twelve power supply pins: AVCC, DVDD, AVDDPLL, VDDS, AVDD and VDDPLL. Refer to Table 1 for the Power supply pin assignments. Refer to Figure 1 for Power Supply Decoupling.

Table 1: Power Supply Pin Assignments for the CH7218 (68QFN)

Pin	# of Pins	Type	Symbol	Description
1, 25, 42, 56	4	Power	AVCC	Analog supply voltage (3.3V)
11, 43	2	Power	DVDD	Digital supply voltage (1.2V)
18	1	Power	AVDDPLL	PLL supply voltage (1.2V)
21, 29	2	Power	VDDS	Serializer supply voltage (1.2V)
59, 65	2	Power	AVDD	Analog supply voltage (1.2V)
1	68	power	VDDPLL	Analog supply voltage (1.2V)
12, 22, 28, 44, 62, Thermal pad	6	Ground	GND	Power ground

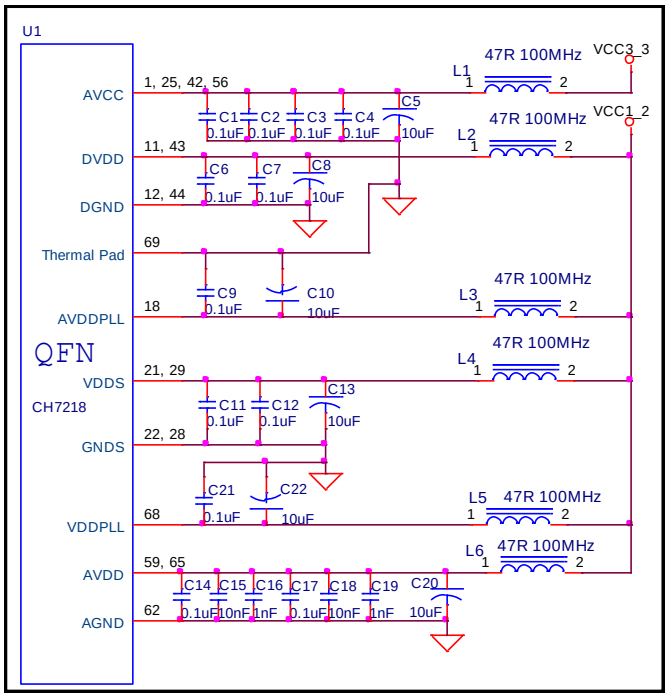

Figure 1: Power Supply Decoupling and Distribution

Note: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ωat 100MHz. Refer to Fair Rite part #2743019447 for details (an equivalent part can be used for the diagram).

2.1.3 On chip power-on reset function's sequence

The power supply must be valid and stable at least 9ms before RB signal become invalid.

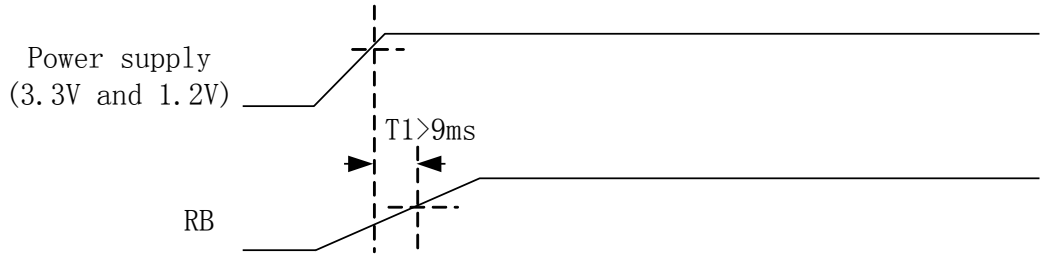

Figure 2: Power on and RB timing

2.2 Internal Reference Pins

• RBIAS pin

This pin sets the swing level of the HDMI outputs. A 1 KΩ, 1% tolerance resistor should be connected between RBIAS and GND as shown in **Figure 3**. A smaller resistance will create larger swing level of the HDMI outputs. The distance between the resistor and the CH7218 should be less than 6mm, the shorter and wider trace the better. For optimal performance, this signal should not overlay the analog power or analog output signals.

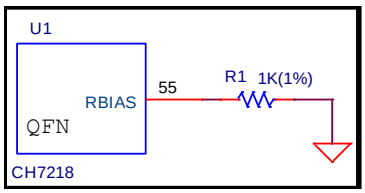

Figure 3: RBIAS Pin Connection

2.3 General Control Pins

• RB

This pin is the chip reset pin for the CH7218. The RB pin is internally pulled-up. But when it is pulled-low, this pin places the device in the power-on-reset condition. As shown in **Figure 4**, one 1MΩ resistor is necessary to be pulled high to 3.3V. One 0.1uf capacitor is recommended to be pulled low to GND. After the powers are stable, send the RB signal (low to high) to the chip, as shown in **Figure 2**.

• XI, XO

A 25MHz crystal (±30ppm) can be connected to XI and XO as the CH7218 the optional reference clock input. In PCB design, a 25MHz crystal must be placed as close as possible to the XI and XO pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates the timing reference for the CH7218, it is essential that noise not couple into these input pins.

The crystal load capacitance, CL, is usually specified in the crystal spec from the vendor. Refer to Figure 4 for a crystal circuit reference design and an example of load capacitors.

CH7218 includes an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7218. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±30 ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±30 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to CH7218 (C_{ext}).

To be able to tune, a variable capacitor may be connected from XI to ground.

Note that the XI and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$\mathbf{C}_{ext} = (2 \times C_L) - C_{int} - 2C_S$

Where
C_{ext} = external load capacitance required on XI and XO pins.
C_L = crystal load capacitance specified by crystal manufacturer.
C_{int} = capacitance internal to CH7218 (approximately 10-15 pF on each of XI and XO pins).
C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

such that $C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int} = 2C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int} /2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

• GPIO0~10, GPIO12

General Purpose Input/Output Interface

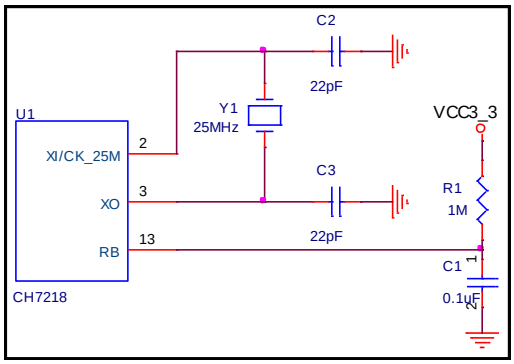

Figure 4: General Control Pins

2.4 Serial Port Control Pins

• SPC0 and SPD0

SPD0 and SPC0 function as a serial interface where SPD0 is the bi-directional data and SPC0 is an input-only serial clock. In the reference design, SPD0 and SPC0 pins are pulled up to +3.3V with 6.8k resistors. Through these two pins, the internal register values of the chip can be read.

• DDC_SC and DDC_SD

DDC_SC and DDC_SD are used to interface with the DDC of DVI/HDMI receiver. This DDC pair needs to be pulled up to 5V through 1.8 KΩ resistors

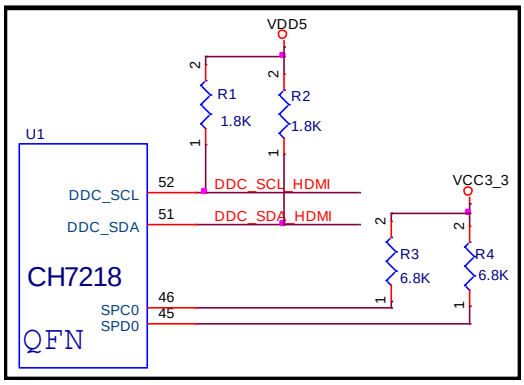

Figure 1: Serial Port Interface

2.5 Display Port Signal Pins

• DP0P/N, DP1P/N, DP2P/N, DP3P/N

These pins accept two AC-coupled differential pair signals from the Display Port transmitter or the Type-C DP Alt. Since the digital serial data of the CH7218 may be toggled at speeds up to 8.1 GHz, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7218 be kept as short as possible, avoid discontinuities in the reference plane and be isolated as much as possible from the analog outputs and analog circuitry. For optimal performance, these signals should not overlay the analog power or analog output signals. When a signal pair has to changes layers, the ground stitching vias should be placed close to the signal vias. A minimum of 1 to 3 stitching vias per pair of signals is recommended. Never route a trace so that it straddles a plane split. It is recommended that 5 mils traces be used in routing these signals. There should be 7 mils spacing between each intra pair. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 50mils. Bend smaller than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH, as shown in Figure 6.

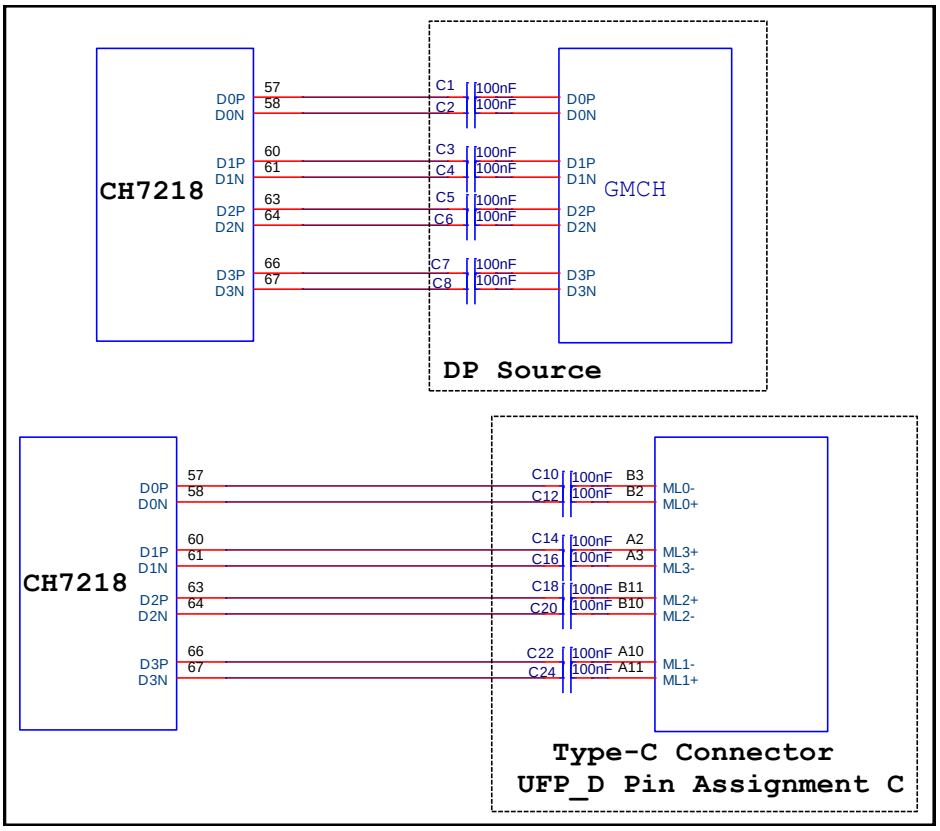

Figure 6: CH7218 DP Main Link Lane or USB Type-C DP Alt Mode Inputs

• AUXP and AUXN

These two pins are for Display Port AUX channel control or USB Type-C DP Alt Mode that accepts a half-duplex, bi-directional AC-coupled differential signal. An AC coupling capacitor, 0.1µF recommended, must be placed on the end as shown in Figure 7.

• AUXP_DET and AUXN_DET

These two pins are for Display Port AUX channel Connection Detection

• HPD_DP

This output pin indicates whether the device is active or not. It also generates an interrupt pulse as defined by the Display Port standard. Output voltage is 3.3V. A resistor, greater than 100KΩ, should be connected between this pin and GND as shown in Figure 7.

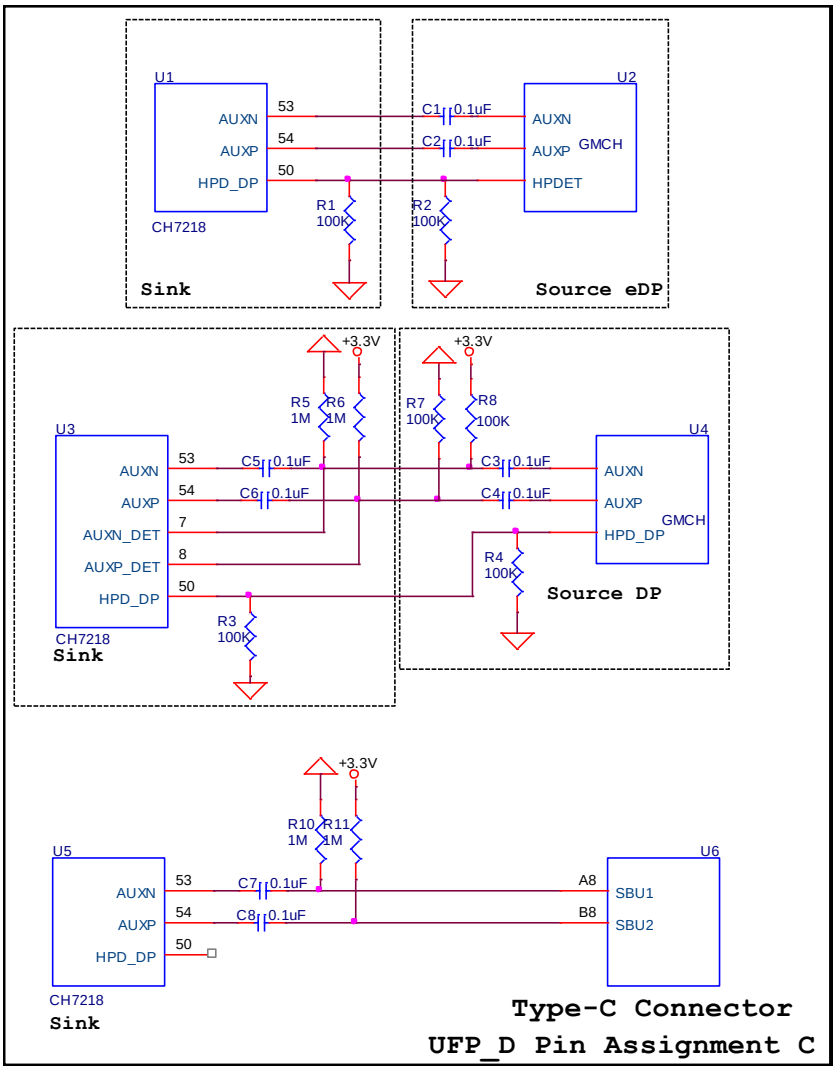

Figure 7: CH7218 AUX channel and HPD_DP

2.6 USB Type-C Signal Pins

• USB0_DN/P

The D+/- input of USB Type-C interface. These pin should be pulled low with 10K Ω or shorted to Ground directly if unused.

• Rd0/Rd1

USB Type-C Dead Battery Rd Resistor, Connect CC0_A or CC1_A to this pin to enable dead battery Rd on CC0_A or CC1_A pin. It can be left open or pulled down to the ground if unused.

• CC0_A/VCONN/VCONN_DET

CC0_A Port A USB Type-C Configure Channel 0.

VCONN Connect this pin to VCONN pin of USB Type-C Plug Connector if CH7218 is used in VCONN Power Accessory mode.

VCONN_DET USB VCONN Voltage Detection, Voltage input 2.7 ~ 5.5v

• Ra

Ra Resistor. When used in typeC accessory mode, this pin needs connect to CC0. It can be left open or pulled down to the ground if unused.

• CC1_A

Port A USB Type-C Configure Channel 1

• GPIO5/CC0_B

General Purpose Input/output or Port B USB Type-C Configure Channel 0

• GPIO4/CC1_B

General Purpose Input/output or Port B USB Type-C Configure Channel 1

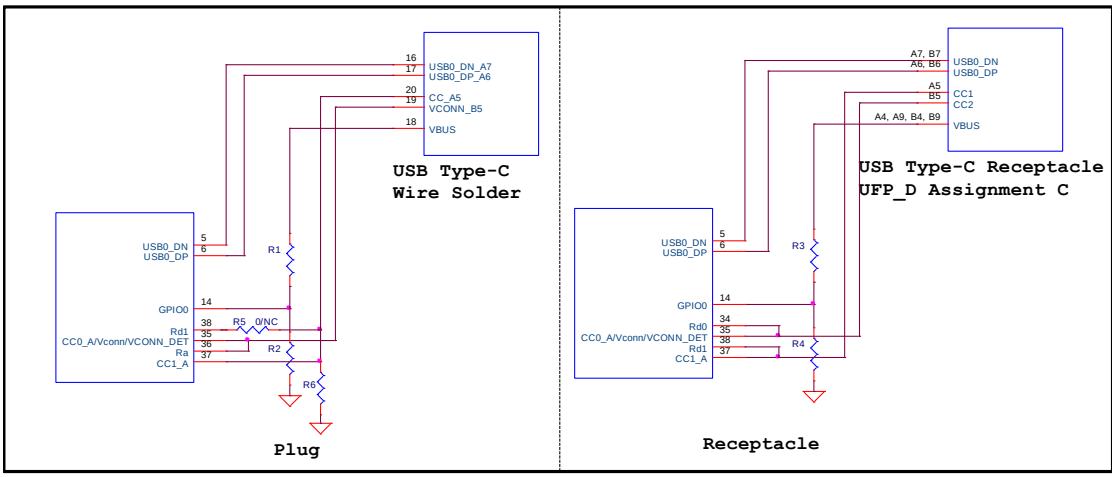

Figure 8: CH7218 Plug and Receptacle Interface

2.7 HDMI Output

The TXCB/TXC, TX0B/TX0, TX1B/TX1, TX2B/TX2 signals are high frequency differential signals that need to be routed with special precautions. Since those signals are differential, they must be routed in pairs.

2.7.1 Differential Pair Impedance

To match the external cable impedance and maintain the maximal energy efficiency it is important to meet the impedance target of 100Ω ± 10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thickness, board dielectric, etc. The HDMI differential pairs should be routed on the top layer directly to the HDMI connector pads if possible.

2.7.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized; inductive effects may be introduced, causing spikes in the signals. The CH7218 should be as close to the HDMI connector as possible. Trace routing lengths from CH7218 to the HDMI connector are limited to a maximum of 2 inches.

2.7.3 Length Matching for Differential Pairs

The HDMI specifies the intra-pair skew and the inter-pair skew as in **Table 2**. The intra-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between the true and complement signals. The inter-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between any two single-ended data signals that do not constitute a differential pair.

Table 2: Maximum Skews for the HDMI Transmitter

Skew Type	Maximum at Transmitter
Intra-Pair Skew	0.15 T_{bit}
Inter-Pair Skew	0.20 T_{Pixel}

Where T_{bit} is defined as the reciprocal of Data Transfer Rate and T_{Pixel} is defined as the reciprocal of Clock Rate. Therefore, T_{Pixels} is 10 times T_{bit}. In other words, the intra-pair length matching is much more stringent than the inter-pair length matching.

It is recommended that length matching of both signals of a differential pair be within 5 mils. Length matching should occur on a segment-by-segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 10 mils.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

2.7.4 ESD Protection for HDMI Interface

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each HDMI output (data and clock).

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel recommended diode protection circuitry, using ALPGA&OMEGA AOZ8S202UD4 diode array devices, will protect the CH7218 device from HDMI transmitter discharges of greater than 8kV (contact) and 10kV (air). The AOZ8S202UD4 have a typical capacitance of only 0.15pF between I/O pins. This low capacitance won't bring too much bad effect on HDMI eye diagram test.

Figure 9 show the connection of HDMI connectors, including the recommended design of AOZ8S202UD4 diode array devices. HDMI connector is used to connect the CH7218 HDMI outputs.

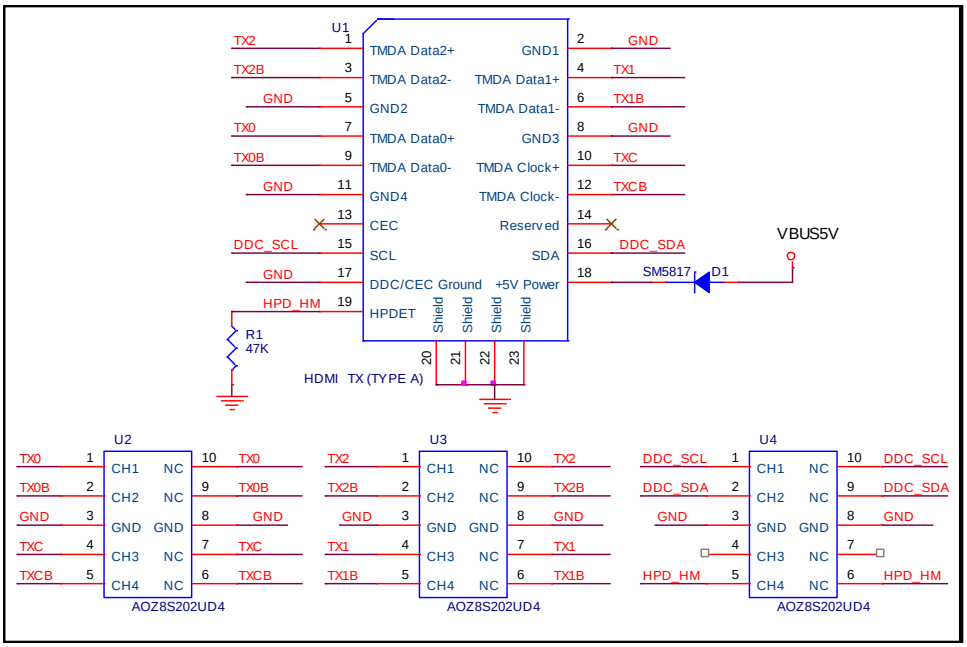

Figure 9: The connection of the HDMI outputs

• HPD_HM

This output pin connects to the GND through a 47KΩ resistor. Refer to **Figure 9** for the design example.

• CEC_HM

HDMI CEC channel

2.8 Thermal Exposed Pad Package

The CH7218 is available in a 68-pin QFN package with exposed thermal pad. The advantage of the exposed thermal pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed thermal pad package provides a means of reducing the thermal resistance of the CH7218. Careful attention to the design of the PCB layout is required for good thermal performance. It is necessary to put thermal vias in the PCB thermal pad, thermal vias are typically used to conduct the heat away from the device and to transfer effectively the heat from the top copper layer of the PCB to the inner or bottom copper layer or to the outside environment. The number of thermal vias is recommended to be more than 16 for maximum heat dissipation, the exposed thermal pad of the package should be soldered to the PCB as shown in **Figure 10**.

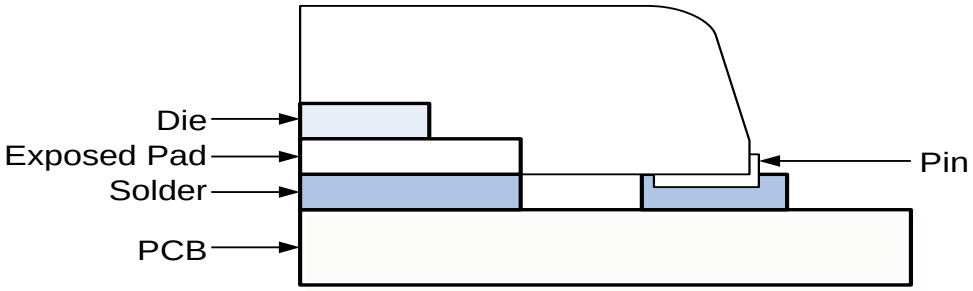

Figure 10: Cross-section of exposed thermal pad package

3.0 REFERENCE DESIGN EXAMPLE

The following schematics are to be used as a CH7218 PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7218 and would like to have a complete reference design schematic should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example

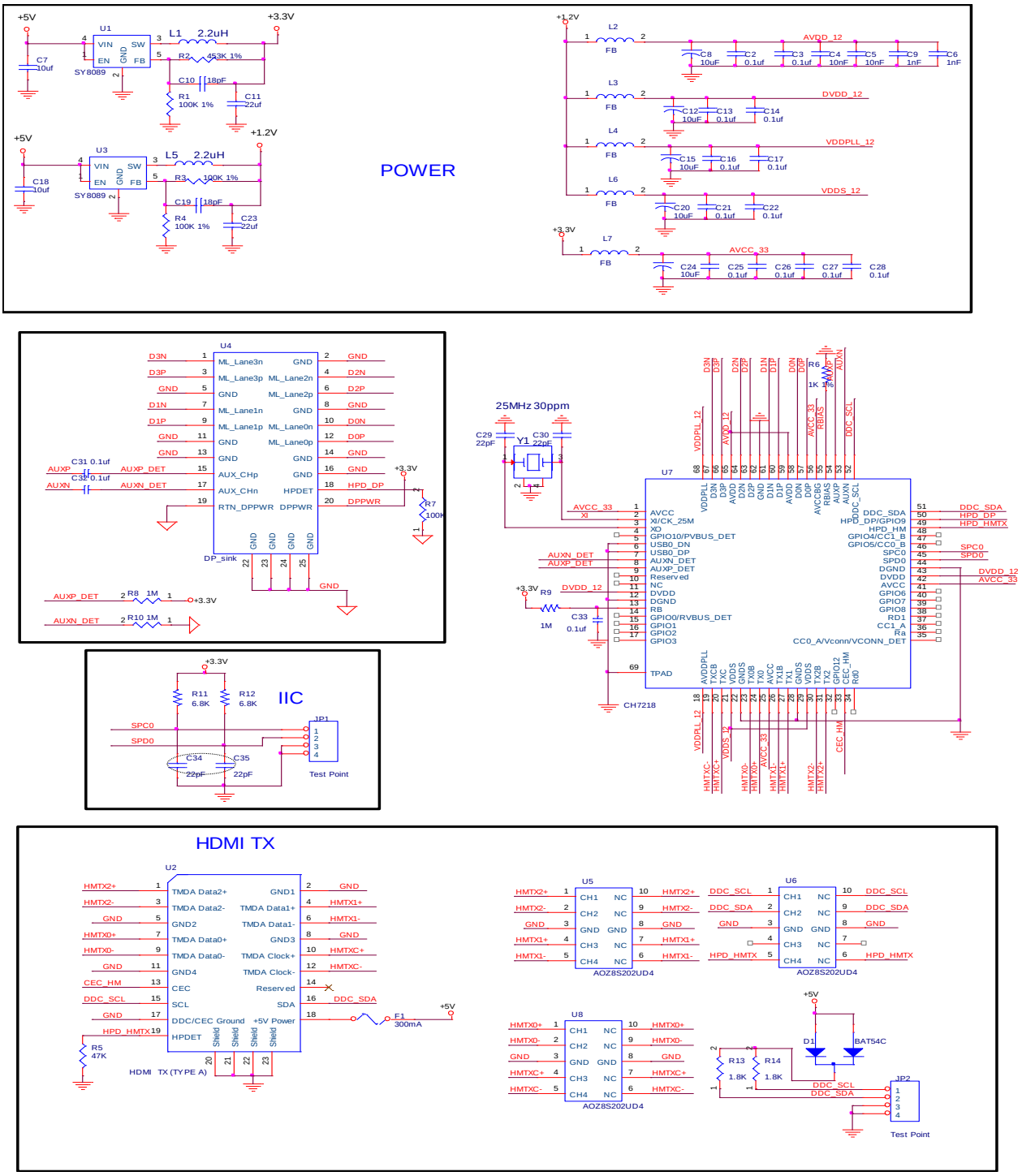

Figure 11: CH7218 DP to HDMI Reference schematic

3.2 Reference Board Preliminary BOM

Table 3: CH7218 Reference Design BOM List

Item	Quantity	Reference	Part
1	15	C2,C3,C13,C14,C16,C17, C21,C22,C25,C26,C27,C28, C31,C32,C33	0.1μF
2	2	C4,C5	10nF
3	2	C6,C9	1nF
4	7	C7,C8,C11,C12,C15,C18, C20,C23,C24	10μF
5	2	C11,C23	22μF
6	2	C10,C19	18pF
7	4	C29,C30,C34,C35	22pF
8	1	D1	BAT54C
9	1	F1	300mA
10	2	JP1,JP2	Test Point
11	1	L1	2.2μH
12	5	L2,L3,L4,L6,L7	FB
13	1	L5	2.2μH
14	3	R1,R3,R4	100K 1%
15	1	R2	453K 1%
16	1	R5	47K
17	1	R6	1K 1%
18	1	R7	100K
19	3	R8,R9,R10	1M
20	2	R11,R12	6.8K
21	2	R13,R14	1.8K
22	2	U1,U3	SY8089
23	1	U2	HDMI TX (TYPE A)
24	1	U4	DP_sink
25	3	U5,U6,U8	AOZ8S202UD4
26	1	U7	CH7218
27	1	Y1	25MHz 30ppm

4.0 REVISION HISTORY

Table 4: Revisions

Rev. #	Date	Section	Description
0.1	09/18/2020	All	Layout Guide and Design Guide for CH7218 release.
0.2	08/18/2021	2.5 2.6 2.7.2 2.7.4 3.1 3.2	Modify the length for inter pairs Delete CC_B Added length limit Modify the ESD component Modify the schematic Modify the BOM
0.3	10/28/2021	2.6 3.1	Modify VBUS_DET to NC Modify Figure 8 Modify the schematic
0.4	01/06/2023	2.8	Add thermal vias requirement
0.5	08/24/2023	2.3 2.6 3.1 3.2	Add C_L Add CC_B Modify the schematic Modify the BOM

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