PCB Layout and Design Guide for CH7515A

1.0 INTRODUCTION

Chrontel's CH7515A is a low-cost, low-power semiconductor device that translates the eDP/DP signal to the LVDS in form of RGB. This innovative eDP/DP receiver with integrated 4 channel LVDS transmitters is specially designed to target the All-In-One and the notebook market segment.

This application note focuses only on the basic PCB layout and design guidelines for CH7515A Embedded Display Port/ Display Port Receiver with LVDS Transmitter. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 128-pin TQFP (14x14mm) package of the CH7515A. Please refer to the CH7515A datasheet for the details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7515A should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C2, C3, C4, C5, C8, C9, C10, C11, C14, C15, C16, C17, C19) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7515A and CH716A ground pins, in addition to ground vias.

2.1.1 Ground Pins

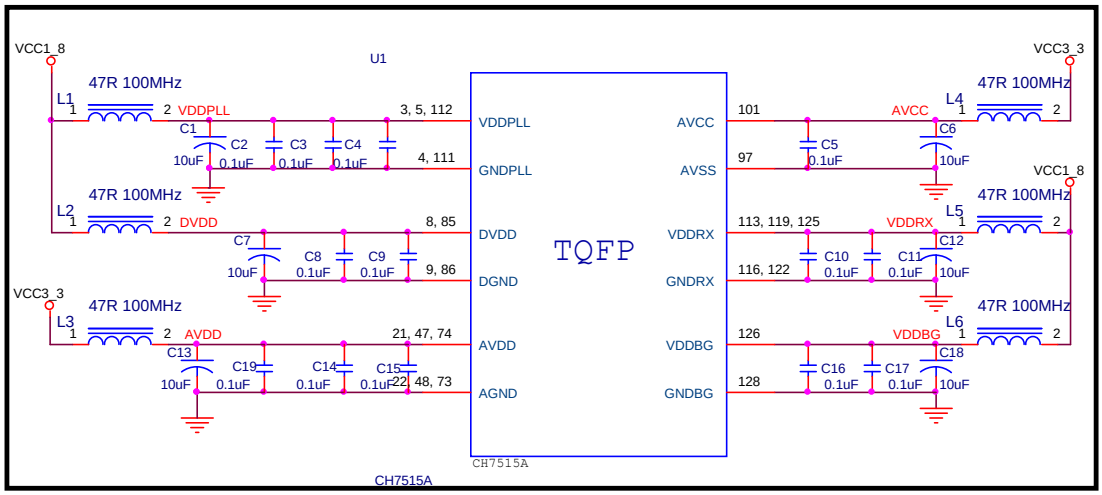
The CH7515A should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7515A ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

The power supplies include VDDPLL, DVDD, AVDD, AVCC, VDDRX, and VDDBG. Refer to **Table 1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7515A (128TQFP)

Pin Assignment	# Of Pins	Type	Symbol	Description
3, 5, 112	3	Power	VDDPLL	PLL Power Supply (1.8V)
4, 111	2	Ground	GNDPLL	PLL Ground
8, 85	2	Power	DVDD	Digital Power Supply (1.8V)
9, 86	2	Ground	DGND	Digital Power Ground
21, 47, 74	3	Power	AVDD	LVDS Power Supply (3.3V)
22, 48, 73	3	Ground	AGND	LVDS Ground
101	1	Power	AVCC	Analog Power Supply (3.3V)
97	1	Ground	AVSS	Analog Ground
113, 119, 125	3	Power	VDDRX	DP Rx Power Supply (1.8V)
116, 122	2	Ground	GNDRX	DP Rx Ground
126	1	Power	VDDBG	Band-gap Power Supply (1.8V)
128	1	Ground	GNDBG	Band-gap Ground



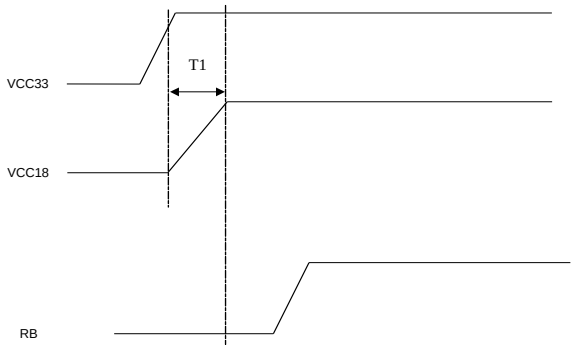


Figure 1: Power Supply Decoupling and Distribution

Note:

1. **Pease make sure the Voltage of AVCC and AVDD (VCC33) should be given earlier than the DVDD and VDDPLL (VCC18).**
2. **The RB signal should be given to CH7515A after the powers are stable.**

3. **T1 (the VCC18 rise slope time) should not be larger than 2ms**
4. **The exposed pad, which is the Thermal pad, must be linked to GND.**
5. **All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05 Ohm at DC; 23 Ohm at 25MHz & 47 Ohm at 100MHz. Please refer to Fair Rite part #2743019447 for details or an equivalent part can be used for the diagram.**

2.2 Internal Reference Pins

• RBIAS pin

This pin sets the Band-gap Bias Voltage. A 10 K-Ohm, 1% tolerance resistor should be connected between RBIAS and GND as shown in **Figure 2**. A smaller resistance will create less Band-gap Bias voltage. This resistor should be placed with short and wide traces as near as possible to CH7515A. For optimum performance, this signal should not overlay the analog power or analog output signals.

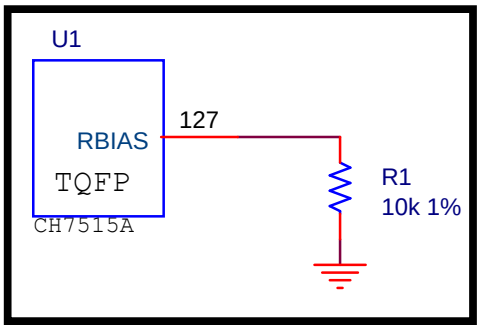


Figure 2: RBIAS Pin Connection

2.3 General Control Pins

• RB

This pin is the chip reset pin for CH7515A. RB pin, which is internally pulled-up, places the device in the power on reset condition when this pin is low. As shown in **Figure 3,** one 10Kohm resistor is necessary to be pulled high to DVDD (1.8V). One 0.1uf capacitor is recommend to be pulled low to GND. After the powers are stable, please give the chip the RB signal (low to high) As shown in **Figure 1**.

Option1: link RB signal to external GPIO_PCH signal (1.8V).

Option2: add the level shifter circuits to link RB signal to GPIO_PCH signal (3.3V).

• XI, XO

27MHz crystal (±30ppm) can be connected to these pins of XI, XO as the CH7515A optional reference clock input. In PCB design, 27MHz crystal must be placed as close as possible to the XI and XO pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7515A, it is very important that noise should not couple into these input pins.

The crystal load capacitance, CL, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors, **Figure 3** shows a reference design for crystal circuit design.

• REFCK

The REFCK is also the optional pin as reference input clock of the CH7515A. The choice is injecting clock 27MHz (3.3V) at this pin as shown in **Figure 3**. For PCB design, the capacitor must be placed as close as possible to the REFCK pin, with traces connected from point to point, overlaying the ground plane.

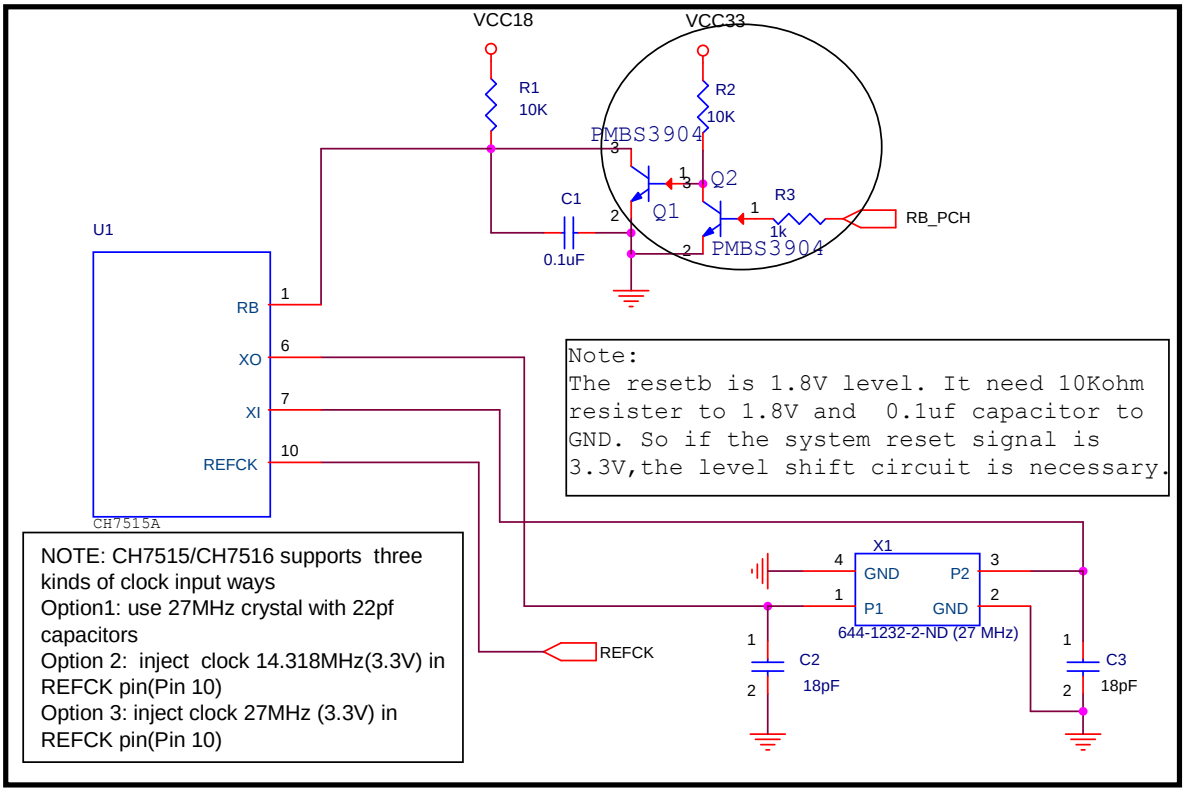


Figure 3: General Control Pins

2.4 Serial Port Control Pins

• SPC0 and SPD0

SPD0 and SPC0 function as a serial interface where SPD0 is bi-directional data and SPC0 is an input only serial clock. In the reference design, SPD0 and SPC0 pins are pulled up to VCC3_3 with 6.8kohm resistors. Through these two pins, the internal register values of the chip can be read and can update the external Boot ROM. These pins should be connecting to SPC1 and SPD1 with Jumpers as shown in **Figure 4**.

• SPC1 and SPD1

SPD1 and SPC1 function as a serial interface where SPD1 is bi-directional data and SPC1 is an input only serial clock. In the reference design, SPD1 and SPC1 pins are pulled up to VCC3_3 with 6.8kohm resistors as shown in **Figure 4**.

SPD1 and SPC1 are used to interface with CH9904 (the serial BOOT ROM). From the BOOT ROM, the EDID and Programmable Registers can be setting in BOOT ROM. When powering up, CH7515A will auto-load the values from the BOOT ROM.

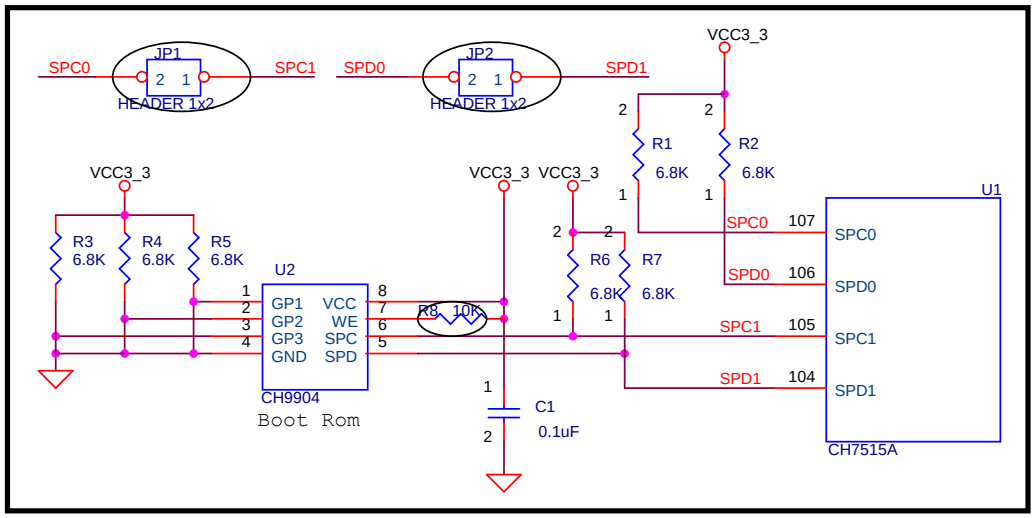


Figure 4: Serial Port Control

Note:

1. Pease make sure the Voltage (3.3V) should be given earlier than the DVDD and VDDPLL.

2. If the SPC0/SPD0 or AUX channel is used to update the CH9904, the precondition is that MCU firmware must work well. We advise that the customers use IIC/SMBUS to update CH9904 by linking IIC/SMBUS to SPC0 and SPD0

2.5 Display Port Signal Pins

• RXP/N0, RXP/N1, RXP/N2, RXP/N3

These pins accept four AC-coupled differential pair signals from the Display Port transmitter.

Since the digital serial data of the CH7515A may be toggled at speeds up to 2.7 GHz, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7515A should be kept as short as possible and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 10mils. Bend, which is smaller than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH, as shown in **Figure 5**

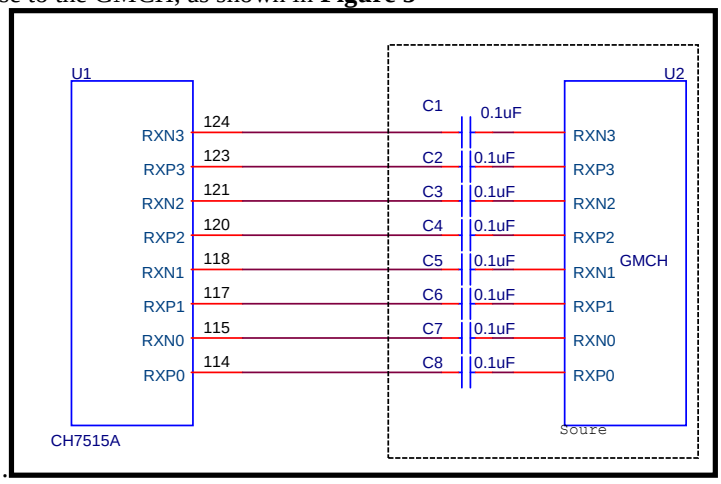


Figure 5: CH7515A DispalyPort Main Link Lane Inputs

• AUXP and AUXN

These two pins are Display Port AUX channel control that accepts a half-duplex, bi-directional AC-coupled differential signal.
They must have the AC-coupling capacitors, and 100nF capacitors are recommended in this document, as shown in **Figure 6**.

• HPDET

This output pin indicates whether this device is active or not. It also generates interrupt pulse as defined by Display Port standard. Output voltage is 3.3V. A resistor more than 100K-Ohm should be connected between this pin and GND, as shown in **Figure 6**.

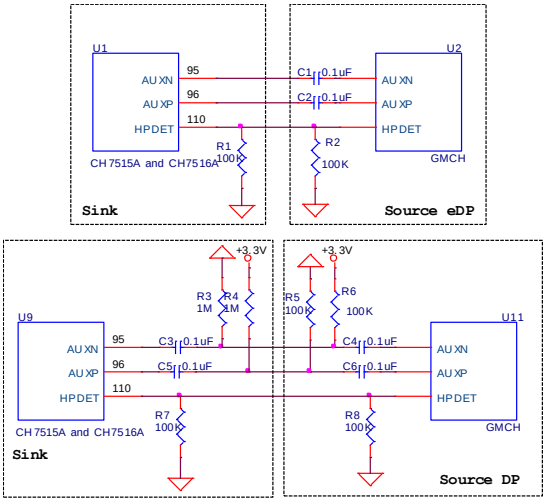


Figure 6: CH7515A AUX channel and HPDET

2.6 LVDS Signal Pins

• LVDS Outputs (LDxP and LDxN, LCxP and LCxN?)

The LVDS output signals are LDxP and LDxN. The LVDS is a differential interface with a nominal swing 200mV. The following rules should be applied to the signals:
1. Keep traces as short as possible.
2. Make these traces have 100-ohm differential impedance.
3. Trace widths should be 5 mils.
4. Intra Pair spacing (spacing between the "+" and "-" pairs) should be 7mils.
5. Inter Pair spacing (spacing between one differential pair and another) should be a minimum of 20 mils exclude pin pitch around.
6. Difference in trace lengths between "+" and "-" pairs should be within 5mils.
7. Difference in trace lengths among Inter pairs should be within 10mils.
8. "+" And "-" pairs should be routed in parallel.

2.7 Audio Output

• IIS
IIS audio output can be configured through programming CH7515A registers. (Refer to **Figure 7**)

• SPDIF
For SPDIF output, CH7515A support audio sample frequencies from 32Khz to 192kHz. (Refer to **Figure 7**)

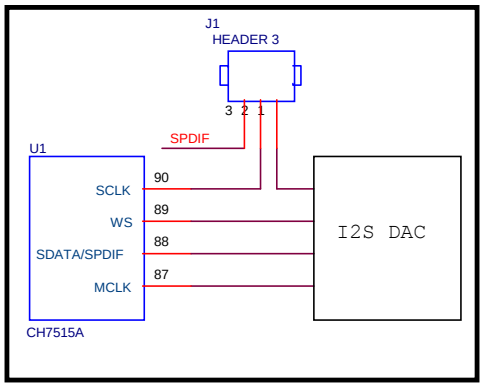


Figure 7: CH7515A IIS or SPDIF Output Pins

2.8 Other function pins

• GPIO [0:3]

These pins are general-purpose input/output. GPIO [0] should be connecting to VDDEN pin with jumper as shown in **Figure 8**.

• BLUP, BLDN

BLUP is the increase backlight brightness input pin.
BLDN is the decrease backlight brightness input pin.
Buttons can be placed at these pins to adjust the backlight brightness. Design is shown in **Figure 8**.

• PWRDN

CH7515A enter into or exits power down state when receiving active low pulse from this pin. The connection is shown in **Figure 8**.

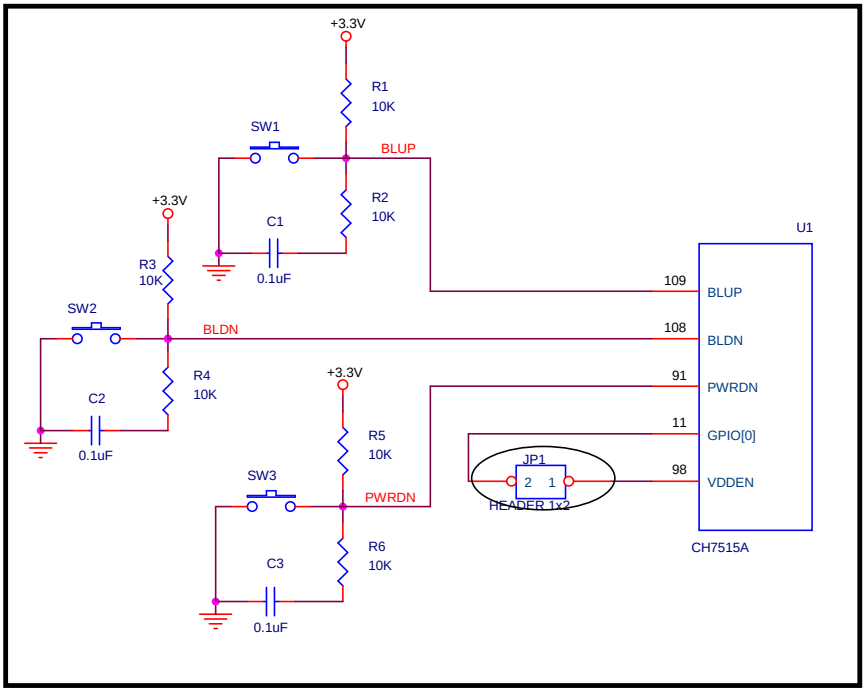


Figure 8: BLDN, BLUP, PWRDN and GPIO [0] Connections

• PSEL [0:2]

These pins can be used as panel select signals. They can be pulled high or low forming into 8 different combinations. Every combination can match with one panel type. The connection is shown **Figure 9**.

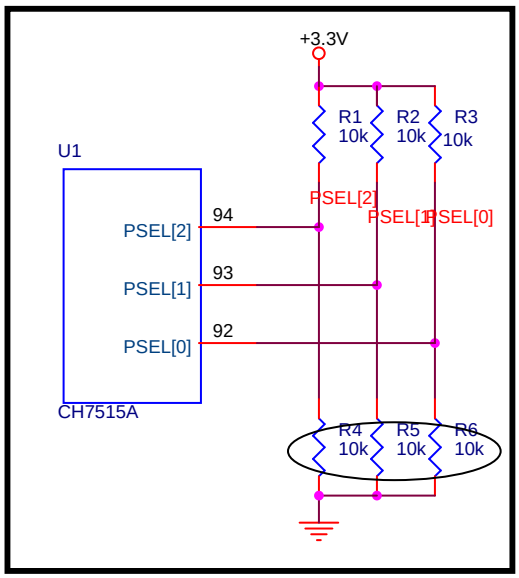


Figure 9: PSEL [0:2] connections

Method 1 (default)

PSEL [2:0] can be connected to high/low level by pull-up/pull-down resistors in CH7515A PCB board; CH7515A can get correct LVDS Panel selection value upon power ON.

Method 2

PSEL [2:0] can be controlled by other chip's GPIO pins in CH7515A application system.

If the chip controlling CH7515A PSEL [2:0] cannot set expected value before CH7515A finishes loading. Its firmware (typically 150ms after CH7515A power ON), then the controlling chip must reset CH7515A to restart CH7515A Loading BOOT ROM file. It is recommended to reset CH7515A by the controlling chip each time LVDS Panel selection value is changed.

The following figure shows the typical cases to control CH7515A PSEL [2:0] by other chip.

Case1 is the right loading case. The PSEL pins can keep stable values in 150ms after the reset signal is given to CH7515A RB pin

Case2 is the wrong loading case. The PSEL pins cannot keep stable values in 150ms after the reset signal is given to CH7515A RB pin. So the RB signal must be given again. The RB pulse width is recommended be larger than 10ms.

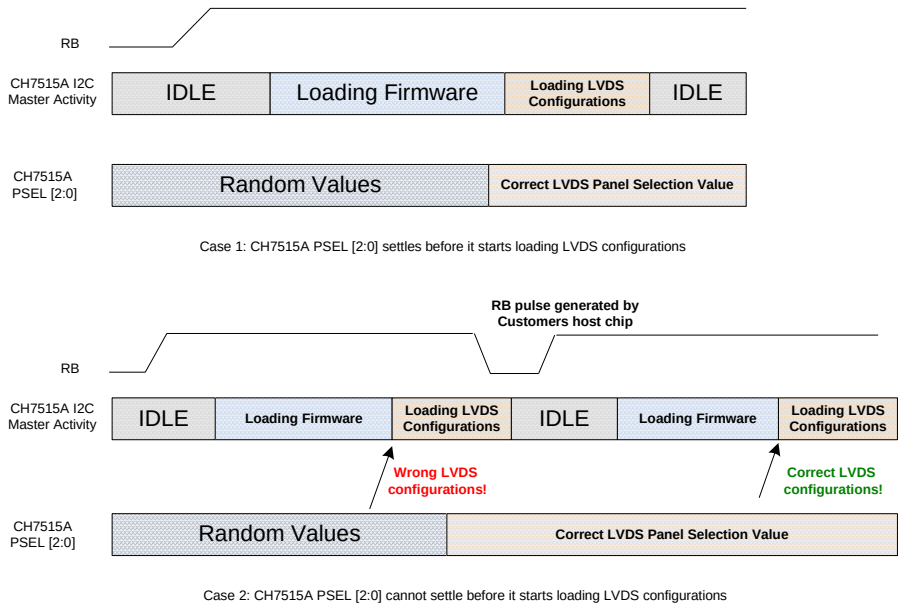


Figure 10: Typical cases to control CH7515A PSEL [2:0] by host chip

Note:
1. The PSEL pins must keep stable values in 150ms after the RB signal is given to CH7515A RB pin. Otherwise, a reset signal must be given again.
2. All the case2 must be finished before VBIOS works. Otherwise, some BIOS pictures will be lost.

• PWM_OUT

The output Frequency from PWM_OUT can be up to 400 KHz. Its duty cycle rang is from 0% to 100%. Or this signal can use PWM bypass mode way to output PWM signal. The voltage level is 3.3V. The detail information can be reference to datasheet.

• PWM_IN

PWM_IN has two work modes: Bypass mode and Duty Cycle Multiplication with AUX CH mode.
In bypass mode, the input frequency to PWM_IN can be up to 1MHz.In Duty Cycle Multiplication with AUX CH mode, the input frequency to PWM_IN can be up to 50 KHz. Despite in which mode, the voltage level is 3.3V.

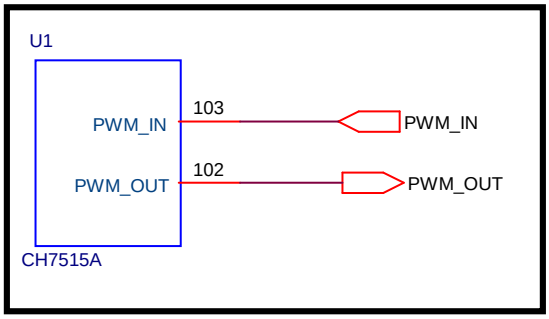


Figure 11: PWM Control connections

• Reserved

Reserved pin (pin 2) should be left open in the application.

2.9 Important Design Considerations

(Panel power, backlight power, pull-up voltage)

• LVDS Power

Close attention must be paid to the power supplied to the LVDS backlight and the LVDS panel. Power requirements may differ from panel to panel. Please check the panels' power and backlight voltage specifications. BLL_EN, BLR_EN and VDDEN of the CH7515A can be used as control signal to turn on the power to the LVDS backlight and the LVDS logic circuitry.

2.10 Thermal Exposed Pad Package

The CH7515A are available in 128-pin TQFP package with thermal exposed pad package. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7515A.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 12.**

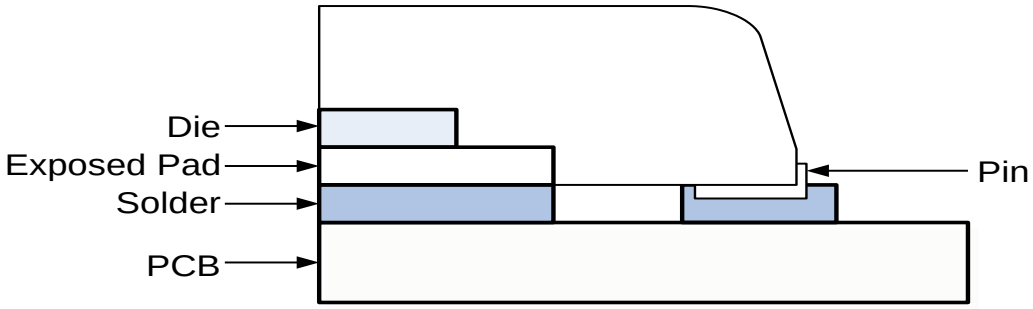
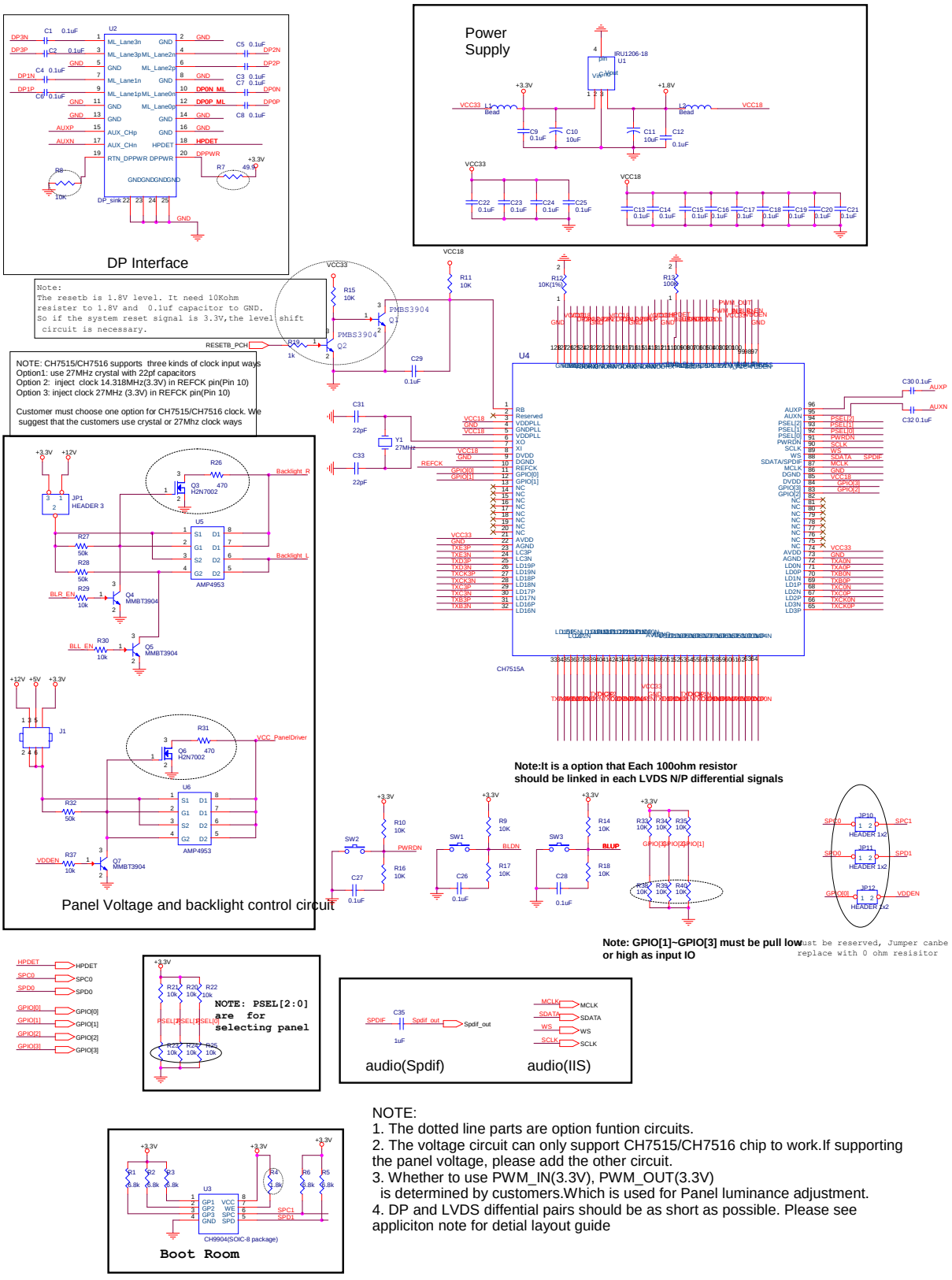


Figure 12: Cross-section of exposed pad package

3.0 REFERENCE DESIGN EXAMPLE

The following schematics are to be used as a CH7515A PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7515A and would like to have a complete reference design schematic, which should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example



NOTE:
1. The dotted line parts are option funtion circuits.
2. The voltage circuit can only support CH7515/CH7516 chip to work.If supporting the panel voltage, please add the other circuit.
3. Whether to use PWM_IN(3.3V), PWM_OUT(3.3V) is determined by customers.Which is used for Panel luminance adjustment.
4. DP and LVDS diffential pairs should be as short as possible. Please see appliciton note for detial layout guide

Figure 13: CH7515A Reference schematic

3.2 Reference Board Preliminary BOM

Table 2: CH7515A Reference Design BOM List

Item	Quantity	Reference	Part
1	29	C1, C2, C3, C4, C5, C6, C7, C8, C9, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C32	0.1uF
2	2	C10, C11	10uF
3	2	C31, C33	22pF
4	1	C35	1uF
5	1	JP1	Header 3
	3	JP10, JP11, JP12	Header 2
6	1	J1	Header 3x2
7	2	L1, L2	Bead
8	2	Q1, Q2	PMBS3904
9	2	Q3, Q6	2N7002
10	3	Q4, Q5, Q7	MMBT3904
11	5	R1, R2, R3, R5, R6	6.8K
12	1	R4	1.8K
13	1	R7	49.9
14	24	R8, R9, R10, R11, R14, R15, R16, R17, R18, R20, R21, R22, R23, R24, R25, R29, R30, R33, R34, R35, R37, R38, R39, R40	10K
15	1	R12	10K 1%
16	1	R13	100K
17	1	R19	1K
18	2	R26, R31	470
19	3	R27, R28, R32	49.9K
20	3	SW1, SW2, SW3	P8058ss-ND
21	1	U1	IRU1206-18
22	1	U2	DP_Sink
23	1	U3	CH9904
24	1	U4	CH7515A
25	2	U5, U6	AMP4953
26	1	Y1	27M

4.0 REVISION HISTORY

Table 3: Revisions

Rev. #	Date	Section	Description
0.1	02/01/2013	All	Initial release
0.2	05/16/2013	2.4	Modify Boot Rom to CH9904
0.3	10/17/2014	2.3 2.4 2.5 2.6 2.8 3.1	Modify crystal name Modify SPC0 and SPD0 schematic Modify Aux schematic Modify LVDS rules Modify GPIO [0] schematic Modify reference schematic
0.4	12/19/2017	2.1	Modify the GND pin
1.0	07/15/2020	All	Remove CH7216A

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